Journal of Information Systems Engineering and Management
2025, 10(11s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Yield Analysis in Semiconductor Manufacturing: Techniques, Case Studies, and Future Direction

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ARTICLE INFO

Received: 09 Nov 2024

Revised: 29 Dec 2024

Accepted: 10 Jan 2025

ABSTRACT

Introduction: This paper aims to provide a comprehensive overview of yield analysis techniques, applications, and future directions in semiconductor manufacturing, highlighting their significance in improving productivity, quality, and competitiveness.

Objective: The scope of this paper includes Techniques Line yield, Die yield, Pareto yield, Functional yield, Parametric yield, Wafer Sort, Fishbone Diagrams, Scatter Plot, Regression Analysis, and Fault Tree Analysis.

Methods: The paper mainly focused on the examination of yield analysis in semiconductor manufacturing, including defect reduction, process optimization, and product quality improvement.

Result: The comprehensive analysis gives an in-depth analysis of yield analysis techniques strengths, weaknesses, opportunities, and threats (SWOT analysis) and their applications. **Conclusion:** Future Research Directions are opportunities for improving yield analysis techniques and their applications.

Keywords: Yield Analysis, SWOT analysis, DMAIC problem-solving steps, yield, design of experiments (DOE) Yield modeling.

INTRODUCTION

Semiconductor manufacturing is a highly intricate, multi-stage process that necessitates the monitoring of numerous interconnected significant process attributes from the early production phases to the final product packaging stage[1]. Wafer fabrication plants employ complex techniques and utilize equipment worth billions of dollars. As technology rapidly advances, semiconductor manufacturers aim to produce defect-less products by adopting advanced fabrication technologies to reduce defect percentage[1], [2]. Key performance indicators (KPIs) like production efficiency, defect density, asset utilization, process duration, and delivery reliability are crucial metrics for evaluating fabrication performances achieving completely defect-free products with cutting-edge technology and maintaining optimal performance metrics is challenging [3]. This is crucial to recognize and evaluate vital process features. Understanding the co-relationship among these parameters as well as modeling their influence on finished goods quality and effective metrics are vital for the industry's success[1], [2].

I. ADVANCEMENT IN SEMICONDUCTOR MANUFACTURING IN RECENT YEARS

The 5G chipset allows faster information transmission. These integrated chipsets transfer data 10 times faster than the 4G[4]. This is the biggest advancement in the communication sector. As well as the global semiconductor industry is also influenced by IoT. It will offer countless opportunities to semiconductor companies. Self-driving vehicles are the biggest achievement in the automotive industry. Which will function with the help of a semiconductor chip[5].

In recent years, AI technology has seen widespread acceptance, allowing enterprises to strategize AI-integrated semiconductor chips[6]. As we see in the early years much advanced research was done in materials. If we talk about new manufacturing methods, the semiconductor industry uses Three-dimensional stacking of device layers. This method substantially enhances chip performance[7]. The choice of AI and Machine Learning in semiconductor chip

design gives precise production because of the ability to quickly process large amounts of data using advanced computing techniques and the creation of large databases containing information on various material's properties and characteristics, creating a new way for machine-learning methods in semiconductor design and manufacturing[6].

II. CURRENT TRENDS IN SEMICONDUCTORS

Extreme Ultraviolet Lithography (EUVL) enables the production of smaller, more complex chips with fewer defects [8].3D Stacked Processors allow for increased performance, reduced power consumption, and smaller footprints[9].Quantum computing is a transformative technology that uses the principles of quantum mechanics to perform calculations and operations on data[10]. Semiconductors play a crucial role in developing quantum computing, enabling faster processing and simulation. Research into new materials like Graphene, Gallium Nitride, and Silicon Carbide enables faster, more efficient, and more powerful chips[11].AI and ML optimize production, predict maintenance, and improve yield[6] .Next-generation process nodes enable even smaller, faster, and more powerful chips. e.g. 5 nm and 3nm[7].Wafer Scale Packaging that allows for increased performance, reduced power consumption, and smaller footprints. Nanoimprint lithography (NIL) is a technique used to fabricate nanoscale structures and patterns on a surface, Enables the production of smaller, more complex chips with fewer defects[12].Sustainable manufacturing refers to the production of goods and services while minimizing environmental impact, conserving resources, and promoting social responsibility[13] .Efforts to reduce waste, energy consumption, and environmental impact in semiconductor manufacturing. These advancements push the boundaries of what's possible in semiconductor manufacturing, driving innovation and enabling new technologies[14]. Integrating EUVL and 3D stacked processors into manufacturing workflow requires innovative wafer fabrication and assembly techniques to maintain yield and efficiency. If we talk about quantum computing, new assembly and packaging methods are needed to handle the unique demands of quantum devices.

While exploring yield analysis, I aim to give details of semiconductor manufacturing processes here. These processes can be broadly segmented into four key stages design, Fabrication, Assembly, and Testing,Figure.1[14].

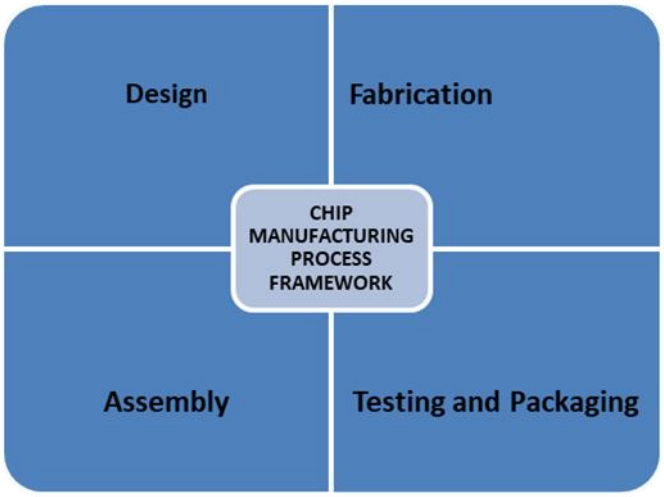

Fig. 1.Chip manufacturing process framework

i) Design - The design stage is the semiconductor manufacturing process's first and most critical phase. It involves creating the blueprint or layout of the integrated circuit (IC) or chip. The steps involved in designing are Digital design, RTL (Register-Transfer Level) design, Synthesis, Physical design, and Mask creation. Design tools used for designing are Electronic Design Automation (EDA) software, Computer-aided design (CAD) tools, and Simulation tools (e.g., SPICE) with the help of these tools, engineers and designers can create, test, and refine their designs more efficiently. After using these design tools, the design engineer can get design output in the form of Netlist, Physical Layout (GDSII file), and Mask patterns. These outputs represent the progression from a circuit's design (netlist) to its physical implementation (physical layout and mask patterns). Each step ensures the accurate transfer of the design onto the semiconductor device

ii) Wafer Fabrication - The semiconductor manufacturing process begins with wafer fabrication. The basic processing

units are provided as a facility. In the fabrication, various layers of metals are constructed on the wafers. This sequence of operations is illustrated in Figure 2. Numerous tough process parameters, which are highly dynamic due to the complexity of the processes, play a crucial role in wafer fabrication[15].

iii) After fabrication, the wafers undergo a process called wafer probe or wafer sort. In this step, each chip on the wafer is ensured to function correctly. Based on the test results, particular code numbers are assigned for the wafers, particularly for those with defective dies, according to the defect type specifications.

Assembly and Packaging - The good chips are separated, wired up, and protected with ceramic shielding.

iv) Final Functional Test - This step is critical to ensure that the chips meet the required standards and will function properly in the devices, they'll be used in. The final test and burn-in process help to, identify any remaining defects or issues, verify the chips' performance and reliability, and provide confidence in the chips' quality before they're shipped to customers.

Semiconductor manufacturing is a complex process that can rapidly produce defective wafers if left unchecked. An accurate yield prediction model serves as a vital warning system enabling proactive measures to maintain quality.

As per the operations sequence shown in the figure.2, good yield management helps wafer makers and manufacturers work together better. It also shows the benefits of improving yield, like reducing waste and increasing efficiency [16]
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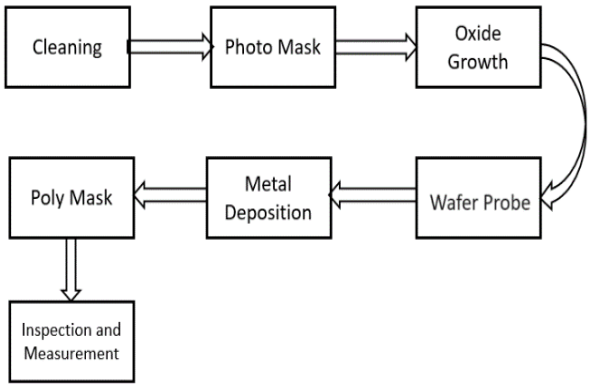

Fig. 2. Operations sequence required on wafers (Chung and Sang 2000)[14]

III. HISTORY AND SIGNIFICANCE OF YIELD ANALYSIS

In semiconductor manufacturing, yield refers to the percentage of non-defective chips produced compared to the maximum number of chips that could be made on a wafer[17].Yield Analysis focuses on examining and understanding the actual yield data from completed production runs. This involves identifying trends, diagnosing issues, and providing insights into the causes of yield loss. The goal is to improve future yields by addressing the identified problems. Yield analysis and enhancement are critical concepts in various fields, especially in semiconductor manufacturing for maximizing production efficiency and profitability.

Accurate yield modeling is critical in today's fast-changing technology environment, as it reveals irregularities between expected and actual yields, and guides data-driven decisions to refine the semiconductor production process. Yield analysis has evolved from basic statistical methods in the 1960s to advanced big data and machine learning techniques today[14].Modern yield analysis integrates data from various sources, including design, manufacturing, and testing, to provide comprehensive insights and drive continuous improvement in semiconductor yields.

TABLE I. DEVELOPMENT OF YIELD ANALYSIS

Years	Development
Late 1960s - Early 1970s	Initial Development Basic Analysis: The initial focus was on understanding basic yield losses and identifying major defect sources. Engineers started using simple statistical methods to analyze defect patterns.

1970s-1980s	Formalization and Technique Statistical Methods: The application of more sophisticated statistical methods and models began to formalize. The Poisson model, which predicts yield based on the number of defects per unit area, became a fundamental tool.
1980s-1990s	Advancements in Tools and Methodologies CAD Tools: The introduction of computer-aided design (CAD) tools allowed for more detailed and accurate modeling of manufacturing processes and yield. These tools helped in the simulation and analysis of potential defect impacts on yield.
1990s-2000s	Integration with Manufacturing Processes Automated Data Collection: The automation of semiconductor fabs allowed for real-time data collection and more sophisticated yield analysis. Statistical process control (SPC) became a standard practice.

OBJECTIVES

Investigate and analyze various yield analysis techniques in semiconductor manufacturing, including Line yield, Die yield, Pareto yield, Functional yield, Parametric yield, Wafer Sort, Fishbone Diagrams, Scatter plots, Regression Analysis, and Fault Tree Analysis. Evaluate the effectiveness of each technique in identifying and addressing yield-related issues in semiconductor manufacturing and examine case studies of successful yield analysis and improvement initiatives in the semiconductor industry.

METHODS

A. Yield Analysis Techniques

To effectively determine and address yield-related issues, several yield analysis techniques can be employed, including Line yield, Die yield, Pareto yield, Functional yield, Parametric yield, Wafer Sort, Fishbone Diagrams, Scatter Plot, Regression Analysis, and Fault Tree Analysis.

line yield is a critical metric in wafer manufacturing, and its analysis is essential for optimizing processes, reducing waste, and improving overall productivity. The line yield calculation considers the number of wafers that enter the process, the number of wafers that are completed, and the number of wafers that are scrapped or reworked. The formulae provided by Cunningham and Horton offer different approaches to calculating line yield, considering factors such as work-in-progress (WIP), cycle time, and rework[14], [18].

a) *Line Yield Analysis:*

$$Line\ Yield\ (\%) = \frac{No.\ of\ wafers\ completing\ the\ process}{No.\ of\ wafers\ entering\ the\ process} \times 100$$

[Using Cunningham's formula]

$$Line\ Yield\ (\%) = \frac{(Actual\ Outputs - Expected\ Outputs)}{(Actual\ Inputs - Expected\ Inputs)} \times 100$$

Change from normal out rate = Variation in wafers out rate Wafers start rate = Number of wafers entering the process Change from normal start rate = Variation in wafers start rate

$$\text{Line Yield } (\%) = \frac{(Processed\ wafer - Scrap\ Wafers)}{(Unprocessed\ wafers)} \times 100$$

[Using Horton's (1998) formula]

Where: Processed wafers = Number of wafers completing the process

Scrap wafers = Number of wafers scrapped or reworked Unprocessed wafers = Number of wafers entering the process.

b) *Die yield*

The wafer sort process is a critical step in semiconductor manufacturing that involves testing individual die (chips) on a wafer using electrical probes. The goal is to identify and separate functional dies from non-functional ones. Die yield, or the yield of functional chips, which goes by other names like wafer sort yield, probe yield, or chip yield. A measure of the fraction of die on a wafer that passes the electrical test and is not discarded. It is an important metric that shows the quality and effectiveness of the wafer fabrication process.

TABLE II. RESPONSIBLE FACTORS FOR DIE YIELD LOSSES

Types of die yield losses	Responsible factors
Functional yield loss: Chips that are faulty and can't perform their intended function	Small Scratch Contamination Other functional failures
Parametric yield loss: Chips that work but are not well enough to meet the specifications.	Lower frequency Low speed Other parametric failures

Die yield losses are crucial for improving the overall yield and ability of the wafer fabrication method. By identifying and addressing the root causes of die yield losses, manufacturers can optimize their processes, reduce waste, and improve productivity.

$$\text{Die Yield} = \frac{(Number\ of\ functional\ die\ on\ a\ wafer)}{(Total\ number\ of\ die\ on\ a\ wafer)}$$

$$\text{Die Yield (\%)} = (\text{Die Yield}) \times 100$$

$$\text{Functional Yield Loss(\%)} = \frac{(Number\ of\ die\ with\ functional\ failures)}{(Total\ number\ of\ Die\ on\ a\ wafer)} \times 100$$

$$\text{Parametric Yield Loss (\%)} = \frac{(Number\ of\ die\ with\ parametric\ failures)}{(Total\ number\ of\ Die\ on\ a\ wafer)} \times 100$$

Overall Yield (%) = Die Yield (%) - Functional Yield Loss (%) - Parametric Yield Loss (%)

c) *Wafer Sort Yield Analysis*

Yield Analysis evaluates the yield of wafers after electrical testing, considering the number of wafers passing the test and the total number of wafers tested.

$$\text{Wafer Sort Yield (\%)} = \frac{Number\ of\ Wafers\ Passing\ Test}{Total\ Number\ of\ Wafers\ Tested} \times 100$$

Where: Number of Wafers Passing Test = Wafers meeting electrical test specifications

Total Number of Wafers Tested = Total wafers undergoing electrical testing

d) *Parametric Yield Analysis*

Parametric Yield Analysis evaluates the yield loss due to parameter variations, such as voltage, current, or frequency, that exceed specified limits.

$$\text{Parametric Yield (\%)} = \frac{(\text{Number of Die meeting Parametric Specs})}{(\text{Total Number of Die})} \times 100$$

Where: Number of Die meeting Parametric Specs = Die with parameters within specified limits

Total Number of Die = Total die on the wafer, including those with parametric failures

Parametric Testing

Measuring electrical parameters of chips to detect performance issues. Parametric testing in semiconductors comprises a series of statistical tests that measure the electrical parameters of semiconductor devices to characterize their performance[19] These tests analyze data assumed to follow a specific distribution, typically a normal distribution, and use parameters like mean and standard deviation to draw inferences. Parametric testing is crucial for semiconductor manufacturers because it can reduce uncertainty in the design process, accelerate product development, and provide historical data for decision-making. It can be applied to various semiconductor devices, including integrated circuits, small-scale integrated circuits, resistors, diodes, transistors, capacitors, and inductors. Additionally, parametric testing is used to monitor wafer-level reliability, develop new wafer process technologies,

and verify existing in-line and end-of-line processes. For instance, when developing a new process, it may undergo a series of tests in a reliability lab that stresses the process under extreme conditions, such as high temperatures and prolonged test periods.

e) *Functional Yield Analysis*

Functional Yield Analysis evaluates the yield loss due to functional failures, such as defects or errors that prevent a die from performing its intended function.

$$\text{Functional Yield (\%)} = \frac{Number\ of\ functional\ Die}{Total\ number\ of\ Die} \times 100$$

Where: Number of Functional Dies = Die that pass functional tests

Total Number of Die = Total die on the wafer,

Including those with functional failures.

f) *Pareto Analysis*

Pareto Analysis is a methodology used to recognize the most common defects or failures in a process. Figure 3 depicts the steps involved in the Pareto analysis

Focus on the small number of defects that have the biggest impact on quality.

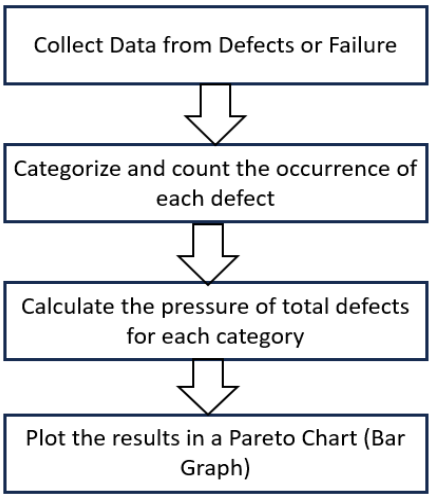

Fig. 3. Steps for Pareto Analysis

g) *Fishbone Diagrams (Ishikawa Diagrams)*

Fishbone Diagrams is a diagram to identify and organize the possible reasons behind a problem as shown in figure.4.

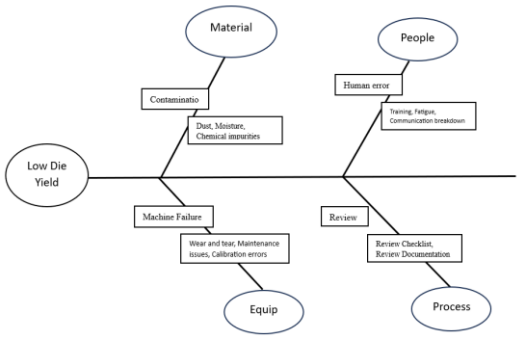

Fig. 4. Fishbone Diagram for Yield Analysis

h) *Scatter Plot Analysis*

This diagram helps to systematically explore and identify potential causes of a problem, guiding further investigation

and corrective action.

Scatter Plot Analysis is a graphical method used to visualize the interrelationship between two variables, identifying patterns, correlations, and potential causes of variation. Following Figure 5. shows the steps in Scatter plot analysis.

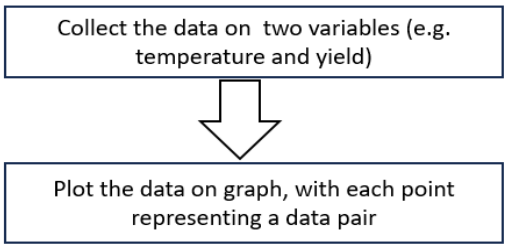

Fig. 5. Steps for Scatter Plot Analysis

i) *Regression Analysis*

Regression Analysis is a statistical method used to set a relation among two or more variables, predicting the value of one variable based on the values of others.

Simple Linear Regression- One independent variable

Multiple Linear Regression- Multiple independent variables

Multiple Linear Regression:

Yield (Y) vs. Temperature (X1), Pressure (X2)

Regression Equation: $Y = 2X1 + 3X2 + 1$

This analysis helps to:

Predict outcomes based on input variables

Identify significant factors affecting a process

Optimize process parameters for improved performance.

j) *Fault tree Analysis*

Fault Tree Analysis is a logical, top-down method used to identify possible failure paths and causes of a system or process failure.

Fault Tree Analysis (FTA) as shown in Figure 6 can be effectively applied to semiconductor yield analysis to identify and prioritize potential failure mechanisms affecting yield. Here's a step-by-step approach to representing FTA in semiconductor yield analysis.

By applying FTA to semiconductor yield analysis, we can: Identify critical failure Identify critical failure mechanisms. Prioritize areas for improvement. Develop targeted solutions to address root causes. Improve overall yield and reduce defects.

k) *Design of Experiment(DoE)*

The high-tech industry like semiconductors is characterized by complex manufacturing processes involving a myriad of factors that influence yield, performance, and reliability. DoE becomes a powerful associate in this field, offering the means to efficiently optimize these processes while minimizing the need for time-consuming trial-and-error methods. Semiconductor manufacturing often involves expensive equipment and materials. DoE aids in uncovering cost-effective approaches by reducing resource consumption and minimizing defects, translating into significant cost savings via knowledge acquisition during the DoE process[20]. DoE helps in identifying factors that influence quality and consistency, enabling manufacturers to produce high-quality chips consistently, and assists in identifying potential risks early in the process, allowing manufacturers to take preventive measures and reduce the likelihood of issues. The semiconductor industry operates in a fast-paced environment, where time-to-market is critical. DoE accelerates product development by rapidly identifying optimal parameters, allowing manufacturers to introduce

cutting-edge devices to the market swiftly.

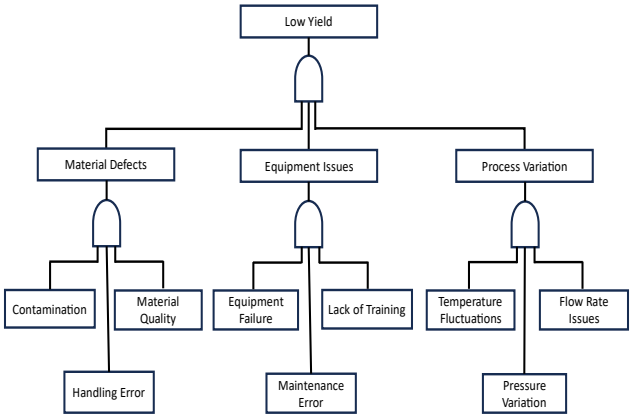

Fig. 6. Fault Tree Analysis

I) Yield Modeling

Yield is a measure of efficiency and quality in production, and in semiconductor manufacturing, it's particularly important because small variations at each stage (wafer, die, and wafer-die interaction) can significantly impact the final output. Yield is a key performance metric evaluated at the wafer, die, and package to assess process performance[21].

Overall yield = Quality of the production line x Quality of the individual chips (wafers). And they are responsible for the product cost. Resources and money can be saved by modeling and predicting these yields accurately. Improve line and chip quality to get more good products out.

B. Ease of Use

As mentioned above, different types of yield analyses as shown in Table III for defect-less production will be used for applications where they are most effective in increasing production.

IV. CASE STUDY

Case studies demonstrate how theories and concepts are applied in real-world scenarios, making them more relatable and substantial. The case study details Six Sigma for Yield Analysis, Contamination on wafers, and Defect inspection which will give the right path for our yield analysis.

A. Six Sigma for Yield Analysis

Six Sigma is a disciplined and data-driven approach focused on enhancing the quality and performance of processes by identifying and eliminating sources of variation and optimizing fluctuations. The primary methodology used in Six Sigma projects is the DMAIC (Define, Measure, Analyze, Improve, Control) problem-solving steps[22].

TABLE III. YIELD ANALYSIS AND THEIR USAGE

Line Yield	This Analysis helps in Early problem detection: Identifying issues early in the manufacturing process reduces the effort and resources required to resolve them. Resource allocation: Analyzing line yield helps direct resources to areas that need improvement. Process optimization: Understanding line yield enables process optimization, lea ding to increased efficiency and reduced waste. Improved productivity: By minimizing losses and rework, line yield optimization can increase overall productivity. Better decision-making: Accurate line yield data informs decisions on process improvements, resource allocation, and capacity planning
Die yield	This analysis helps identify areas for improvement in the wafer fabrication process to increase overall yield and reduce losses

Functional Yield Analysis	This analysis helps identify the percentage of dies that function correctly, indicating the effectiveness of the wafer fabrication process in producing functional devices
Parametric Yield Analysis	This analysis helps identify the percentage of die with parameters within specified limits, indicating the impact of parametric variations on overall yield.
Wafer Sort Yield Analysis	This analysis helps identify the percentage of wafers meeting electrical test specifications, indicating the quality and reliability of the wafer fabrication process
Pareto Analysis	This analysis identifies the top 20% of defects that cause 80% of problems. Focus efforts on addressing these critical few defects
Fishbone Diagrams	This analysis primarily identifies and systematically analyzes the root causes of a problem or issue within a process or system. It is a visual tool that helps teams break down and organize possible causes of a problem, categorizing them into key areas such as people, methods, machinery, materials, measurements, and the environment.
Scatter Plot Analysis	This analysis helps to identify potential causes of variation as well as optimize process parameters. Improve process control and yield.
Regression Analysis	Predict outcomes based on input variables and identify significant factors affecting a process as well as optimize process parameters for improved performance.
Fault Tree Analysis	Identify critical failure mechanisms and prioritize areas for improvement. They develop targeted solutions to address root causes, improve overall yield, and reduce defects.

Figure. 7 Explains a step approach to DMAIC to solve problems in Six Sigma

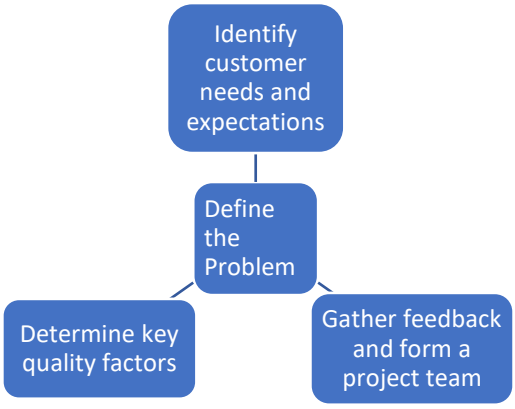

Fig. 7. Define step

Clearly defining the problem and project scope as well as establishing a budget and timeline are the key parameters for a successful process.

The following figure.8 shows the measuring steps for Six Sigma yield analysis.

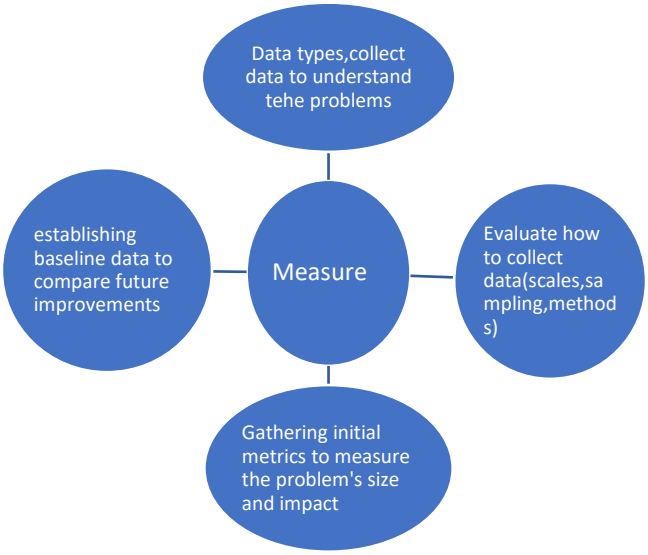

Fig. 8. Measure step

The following figure. 9 shows the basic building blocks of the analysis steps.

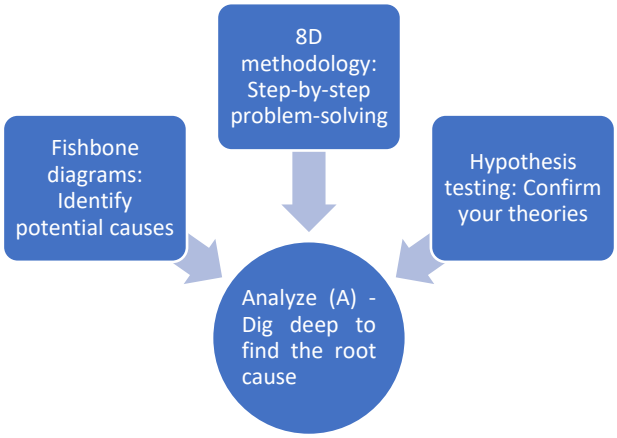

Fig. 9. Analyze Step

Root cause analysis helps to uncover the underlying reason. Figure. 10, Figure 1.1 and Figure. 12 shows the improved steps and control steps and influencing factors in Six Sigma yield analysis.

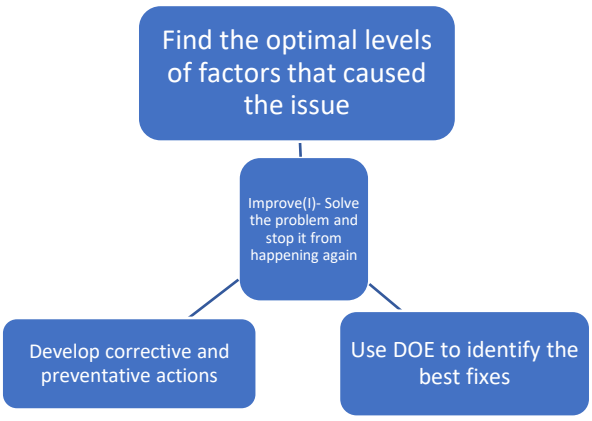

Fig. 10. Improve step

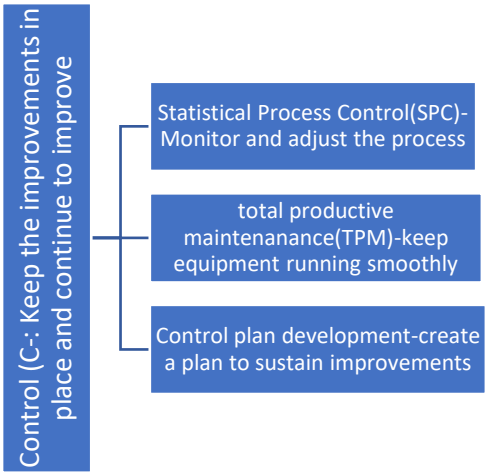

Fig. 11. Control step

Maintain control over the process to prevent slipping back

And reduce fluctuations and defects.

Continuously look for ways to improve and adjust as needed for development[22].

Using Six Sigma to reduce defects in semiconductor manufacturing and improve the final product yields is the most important goal for any semiconductor fabrication[22]

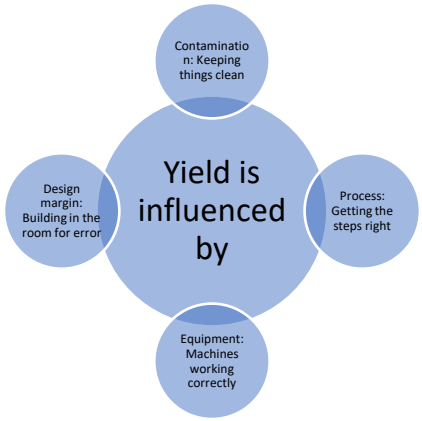

Fig. 12. Influencing Factors on Yield

Six Sigma's DMAIC approach helps control quality and reliability by finding and fixing random defect sources like equipment, processes, materials, and environment. Using 30 years of data from ICE to improve performance.

DMAIC methodology improves quality and reliability by Identifying equipment, process, chemical, and cleanroom issues. Due to the advancement in automation and artificial intelligence, minimizing human contact in handling wafers is possible. Contamination sources in cleanrooms include People- skin, hair, clothes, breath, and sweat. Environment-air, surfaces, equipment, materials, water, and cleanroom sources of contamination have gradually decreased because of the advanced training in this field. To achieve operational efficiency and high-quality chips, fabs must systematically address yield losses and implement key business processes like document control, training, and continuous improvement. Maximize fab efficiency and chip quality by Using a structured approach to resolve yield losses and establishing essential processes like document control, training, and audits with the help of Six Sigma DMAIC methodology, it is possible to improve business processes[22].

B. *Contamination on wafers*

Contamination on a silicon wafer is when something unwanted gets onto or inside the wafer. This can be tiny solid particles (like dust or dirt), ions (tiny, charged particles), or liquid droplets. The mechanism of contamination of silicon wafers is summarized in Figure 8 [23].

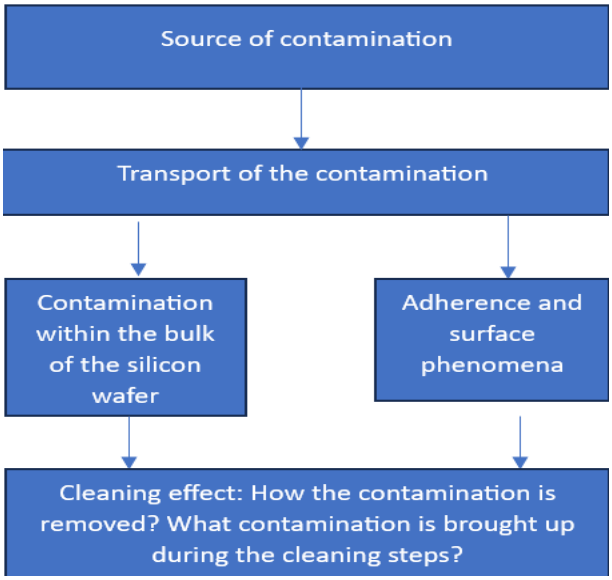

Fig. 13. Contamination Workflow

Contamination workflow- Defect density is a critical metric in semiconductor manufacturing, as it directly impacts the number of usable chips produced. Especially for sub-micron designs, where even small defects can significantly impact device functionality. This is the reason for investing in measuring defect density has increased in recent years for improving the quality and yield of semiconductor manufacturing. By using in-line defect inspection, we can predict yield and improve yield learning which will be helpful for new products for faster identification and address defects, ensuring faster time-to-market. For each node generation where each new node generation brings smaller, more complex designs, defect inspection becomes crucial to maintaining or improving yield. With the help of in-line defect inspection, we can reduce defects, improve quality, and increase the overall yield of the semiconductor products [16], [23].

RESULT

C. Defect inspection

Three types of inspection tools help analyze defect density:

i. Bright Field: Uses regular light for larger defects

ii. Dark Field: Uses special light for smaller defects

iii. SEM: Uses a powerful microscope for tiny defects[6], [23].

Bright-field inspection tools -These Tools use standard or UV light to detect various types of defects on semiconductor wafers with sub-micron designs. They are sensitive to even slight image differences and provide a clear contrast to help the inspection tool capabilities and sampling strategy, the defect size, and the killer ratio calculation for each defect type will improve the confidence level of yield prediction to identify defects, ensuring high-quality semiconductor manufacturing.

Darkfield inspection tool - Uses a laser to illuminate the wafer from a shallow angle, creating a dark background that highlights surface defects. Will detect easily surface defects such as scratches, contaminants, particles, and other surface irregularities[23].

Scanning Electron Microscope (SEM) inspection tool. These tools use advanced microscopy to detect small defects on semiconductor wafers by comparing images between adjacent dies. They provide detailed defect information, classify defects, and can improve defect analysis efficiency by filtering out non-critical defects.

The defect size distribution in semiconductor manufacturing inspection is influenced by three key parameters:

i. Image filtering: The process of refining the image to enhance defect visibility.

ii. Detection threshold: The sensitivity level set to detect defects.

iii. Pixel size: The smallest unit of measurement used to compare images of dies (tiny pieces of semiconductor material). It helps identify defects. Defect size distribution is a critical concept in yield analysis, as it helps predict the likelihood of defects occurring in a manufacturing process. Defect size distribution refers to the statistical distribution of defect sizes in a manufacturing process. It describes the probability of finding defects of different sizes, typically measured in micrometers (µm) or nanometers (nm). The defect distribution law is a mathematical formula that shows how many defects of different sizes are likely to occur. It's like a map that helps us understand where defects are most likely to happen[23].

$D = A / X^n$

Where:

- D is the number of defects (particle count)

- X is the defect size

- A and n are constants (with an often around 3)

A log/log graph will give a straight line where the slope is n.

Corrective factors can be used to modify predictions, but this method has its limitations. More accurate predictions can be achieved by using software that includes design descriptions for all layers of the product, meaning the software has detailed information about the product's design, including all its layers and features. Adopting modulization of defect density, which means the software models and simulates defect density (the number of defects per unit area) for each layer and feature, taking into account various factors that affect defect density. By using this software, manufacturers can get a more accurate prediction of yield, which is critical for optimizing production and minimizing waste[23].

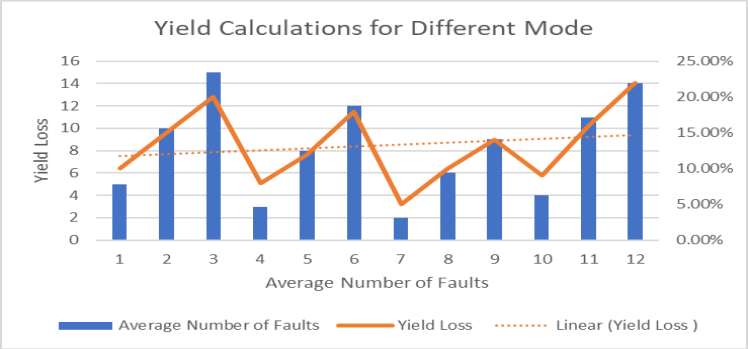

Fig. 14. Yield Calculations from Different Models

Using data to mitigate losses enables a focused effort to tackle problems promptly a manufacturer used to estimate losses manually every month, but now they use a data analytics tool to reduce waste of materials, improve customer quality increase overall production capacity. They also created a special tool to detect and estimate false rejects (good products mistakenly marked as defective) using a pattern recognition algorithm. This tool provides a daily report of false rejects, helping the manufacturer to identify issues quickly, take corrective action, and improve overall efficiency. This approach is a big step in improving semiconductor manufacturing technology[23].

V. SWOT ANALYSIS

Based on Yield Analysis, each technique has its strengths, weaknesses, opportunities, and threads called a SWOT ANALYSIS. The following table shows a SWOT analysis for different analysis techniques which gives proper direction for yield management.

TABLE IV. SWOT ANALYSIS FOR DIFFERENT YIELD ANALYSIS

Analysis Techniques	Strength	Weakness	Opportunities	Threads
Line Yield	Measures overall manufacturing efficiency	Doesn't identify specific failure points	Improving line yield can increase overall productivity	May not account for external factors affecting yield

Die Yield	Focuses on individual die performance	May not account for systemic problems	improving die yield can increase overall wafer yield	May not account for variations in wafer processing
Pareto Yield	Identifies most common failure modes	May oversimplify complex issues	Improving top failure modes can significantly impact yield	May not account for rare but critical failure modes
Functional Yield	Measures yield based on product functionality	Can be difficult to define and measure	Improving functional yield can increase customer satisfaction	May not account for systemic or process-related issues
Parametric Yield	Measures yield based on specific parameters	Can be difficult to define and measure	Improving parametric yield can increase overall product quality	May not account for functional or systemic issues
Wafer Sort	Identifies defective diseases early in the process	May not account for systemic or process-related issues	Improving the wafer sort technique can increase overall productivity	May not account for variations in wafer processing
Fishbone Diagram	Visualize complex relationships between variables	Can be subjective and dependent on user expertise	improving fishbone diagram analysis can increase problem-solving efficiency	May not account for rare or unexpected failure modes
Scatter Plot	- Visualize relationships between variables	- Can be difficult to interpret and analyze	Improving scatter plot analysis can increase process understanding	May not account for complex or nonlinear relationships
Regression Analysis	Quantify relationships between variables	Can be difficult to interpret and analyze	Improving regression analysis can increase process optimization	May not account for rare or unexpected events
Fault Tree Analysis	Visualize complex failure modes and relationships	Can be subjective and dependent on user expertise	Improving fault tree analysis can increase problem-solving efficiency	May not account for rare or unexpected failure modes

DISCUSSION

Conclusion -This paper has comprehensively explored various yield analysis methods, including Line yield, Die yield, Wafer sort yield analysis, Parametric yield analysis, Functional yield analysis, Pareto analysis, Scatter plot analysis, Regression analysis, and Fault tree analysis. Furthermore, we have demonstrated the application of Six Sigma's DMAIC (Define, Measure, Analyze, Improve, Control) framework in yield analysis, highlighting its effectiveness in identifying and addressing defects. The integration of defect inspection techniques has also been shown to enhance the yield analysis process. The findings of this study suggest that a combination of yield analysis methods, Six Sigma's DMAIC approach, and defect inspection techniques can significantly improve defect detection, reduce waste, and enhance overall yield. Future research directions may include, Exploring the application of advanced analytics and machine learning techniques in yield analysis. Investigating the impact of Industry 4.0 technologies on yield analysis. Developing more efficient defect inspection techniques. By adopting the methodologies outlined in this paper, organizations can optimize their yield analysis processes, leading to improved product quality, reduced costs, and increased competitiveness.

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