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Advancing At-Speed Testing through Launch-on-Extra-Shift Architecture

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ABSTRACT

At-speed testing of integrated circuits presents a fundamental challenge in balancing comprehensive fault detection with power management and manufacturing yield optimization. Traditional testing methodologies force designers to compromise between test quality and power constraints, as patterns optimized for fault coverage often generate excessive switching activity that causes voltage drops and false test failures. This article explores the implementation of launch-on-extra-shift testing architecture combined with strategic power management techniques to address these competing requirements. The article examines two primary launch mechanisms for generating test transitions: launch-off-capture, which provides relaxed timing requirements but requires computationally intensive sequential pattern generation, and launch-on-extra-shift, which enables faster combinational pattern generation but introduces stringent timing constraints on scan enable signals. A sophisticated mixed-testing architecture is presented that employs pipelined scan enable structures and dynamic control capabilities through test point integration, allowing different design regions to operate under different launch mechanisms based on their specific characteristics. To mitigate the elevated switching activity inherent in launch-on-extra-shift testing, strategic clock gating techniques are implemented through a hierarchical power management infrastructure that selectively activates or deactivates circuit portions during test operations. The implementation strategy incorporates simulation-based analysis to identify power hotspots and validate design modifications through iterative refinement processes. By combining these architectural innovations with partition-based testing approaches, the methodology achieves enhanced transition fault coverage while maintaining acceptable power profiles and manufacturing economics, demonstrating that temporal and spatial separation of testing activity can preserve pattern quality while reducing instantaneous power consumption without sacrificing fault detection capabilities.

Keywords: At-Speed Testing, Launch-On-Extra-Shift, Power Management, Clock Gating, Transition Fault Coverage

Introduction

At-speed testing of integrated circuits is a fundamental issue in current semiconductor manufacturing: it is necessary to detect all faults, at the same time controlling power consumption and manufacturing yield. The conventional testing methods usually require the designer to decide between the quality and power of the test, and patterns based on covering the fault tend to result in too much switching that results in voltage drops and false test failures. Defects associated with timing have become one of the most important reliability issues in the production of semiconductors due to the complexity of modern integrated circuits with millions of transistors and progressively denser interconnections between transistors. Studies have found that delay defects that do not affect functionality but run the risk of timing violations in certain conditions of operation are a particularly insidious type of fault and necessitate complex detection paradigms. This design/testability power

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ratio has motivated the creation of novel design-for-testability architectures that permit good quality testing without impacting chip reliability or manufacturing economics.

Poor at-speed testing policies have an economic spread across the entire semiconductor supply chain, which influences manufacturing yield and the long-term reliability of products. These methods have been modified, as explained in studies about built-in self-test methodology [1], to deal with delay fault diagnosis in field-programmable gate arrays and application-specific integrated circuits. They acknowledge that traditional stuck-at fault models are inadequate to identify timing-based defects, which can only be detected at certain frequencies of operation and environmental conditions. The shift in the simple fault models to in-depth delay testing involves having complex test pattern generation algorithms that are able to generate patterns that would stress critical timing paths, with management of the power consumption level during testing execution. Research has suggested that loss of yield due to tests can be measured in percentage points of otherwise operating devices in high-performance designs, which has serious revenue implications in the context of large-volume production.

Power-conscious test methodologies have become essential facilitators of quality measures of tests as well as tolerable economics of manufacture. These tools need to be specifically aimed at timing-based delay testing. Research indicates that the small delay defects typically missed by the traditional testing mechanisms, but leading to reliability failures once in the field, are the targets of these tools [2]. Such defects may be as small as a few percent of the clock period and necessitate test patterns that can initiate and record transitions with very fine timing resolution and which do not cause exasperating amounts of switching noise that might obscure the real defects by causing test-induced voltage variations. The methodology should trade off several conflicting goals: completing the transition fault coverage to identify performance-based defects, limiting the maximum power usage during the launch and capture cycles to avoid infrastructure-drop-based failures, supporting reasonable pattern counts to manage test time and test costs, and being compatible with existing design flows and manufacturing test equipment. The development of the launch mechanisms and control architectures is the industry's reaction to these complex demands and allows elaborate testing strategies to maintain fault detection, but work with severe power constraints required to produce modern, inexpensive integrated circuits on the high-yield scale.

Launch Mechanisms in At-Speed Testing

At-speed testing is based on two main mechanisms of generating test transitions, with different trade-offs in terms of implementation complexity, pattern generation efficiency, and timing requirements. Launch-off-capture method. The transitions are triggered by functional logic responses, in which the initial capture clock pulse is derived from the functional output of the last shift cycle. This approach allows slack timing restrictions on scan enable signals because the scan enable transition is not required to take place within the critical timing window of the launch operation and the capture operation. The timing margin available to scan enable deassertion may be significantly more than one functional clock period, usually several nanoseconds of set-up time before the launch pulse. Nevertheless, this flexibility is quite costly in terms of computational requirements since the algorithm involves sequential pattern generation systems that need to account for the logic behavior and state dependencies of multi-cycle systems. As explained in a study of scan-based transition fault testing [3], the software implementation issues with launch-off-capture testing are due to the requirement to produce patterns that can effectively initialize the state of the circuit and, at the same time, launch transitions through the critical paths. The sequentiality of the algorithm tends to generate larger sets of patterns, because each pattern needs to consider the state transition that needs to take place to achieve a set of launch conditions, which may compromise the test application time and cost of

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manufacture. The sequential computation of test pattern generation is particularly hard in large-scale designs where the state space size increases exponentially with sequential elements.

The launch-on-extra-shift approach has its own unique benefits, as it obtains launch patterns as a direct result of scan shift operations, which essentially changes the timing constraint as well as the pattern generation nature. The last shift cycle is also the last shift operation, and the at-speed launch pulse, followed by a capture cycle, a functional clock period later. This two-way cycle does not require intricate state-initialization sequences, with the pattern of launching being automatically enforced by the contents of the shifted scan chains. This method allows the exploitation of the combinational pattern generation engines, which are far faster and more efficient, and in practice can often achieve pattern generation speeds that are many times higher than sequential algorithms. As per research done on the generation of compact test sets [4], test sets generated using combinational approaches can have high fault coverage with a lower number of patterns because it emphasizes efficient propagation of faults through combinational logic paths. The described methodology shows that it is possible to have complete test sets of various faults by using systematic combinational analysis, which can identify patterns that can be used to detect multiple faults. This is due to the reduced fault propagation and fault analysis that is simplified as the test generation algorithm does not need to utilize multi-cycle sequential behavior, but only the single-cycle combinational paths. There is, however, a price to this efficiency and that is it introduces strict timing constraints on scan enable signals, since the scan enable needs to be switched off the shift mode and onto the capture mode during a single functional clock period. This timing limit is especially problematic when used with designs that run at frequencies above several hundred megahertz, because the scan enable signal has to travel over some potentially long routing and drive a large number of flip-flops spread over the chip. This necessitates careful architectural considerations such as pipelined scan enable registers, to manage timing closure across long signal paths, where the pipeline stages introduce controlled delays that align the scan enable transitions with the local clock domains while maintaining the precise timing relationships required for valid at-speed testing.

Parameter	Launch-Off-Capture (LOC)	Launch-On-Extra-Shift (LOES)
Timing Requirements	Relaxed scan enables timing (several nanoseconds margin)	Stringent scan enables timing (single clock period)
Pattern Generation Algorithm	Sequential ATPG engine	Combinational ATPG engine
Computational Complexity	High (exponential state space growth)	Low (single-cycle path analysis)
Pattern Generation Speed	Slower	Significantly faster
Pattern Count	Larger (due to state initialization)	Reduced (efficient fault detection)
Test Application Time	Higher	Lower
Launch Pattern Source	Functional logic response	Scan shift operation
State Initialization	Complex multi-cycle sequences required	Emerges naturally from shifted scan chains
Critical Path Coverage	Requires specific state transitions	Direct combinational path targeting

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Design Frequency Support	Suitable for all frequencies	Challenging for >several hundred MHz
Architectural Requirements	Standard scan architecture	Pipelined scan enables registers needed
Fault Detection Efficiency	Moderate (single fault per pattern typical)	High (multiple faults per pattern)

Table 1: Comparative Analysis of At-Speed Testing Launch Mechanisms [3, 4]

Design Architecture for Mixed Testing

Supporting both launch mechanisms within a single design requires sophisticated control structures that can dynamically accommodate the distinct timing and operational requirements of each testing approach. A pipelined scan enables architecture forms the foundation of this dual-mode capability, where an external scan enable signal generates an internally delayed version through pipeline registers strategically distributed throughout the design hierarchy. This delay allows adequate setup time for downstream logic while maintaining the timing integrity required for at-speed operations, effectively decoupling the external test interface timing constraints from the internal at-speed timing requirements. Research on scan-based transition testing methodologies [5] has established that managing timing constraints in at-speed testing requires careful consideration of signal propagation delays and setup time requirements across diverse circuit topologies. The pipelined architecture also facilitates clock domain crossing management, where different regions of the design operating at different clock frequencies can receive appropriately timed scan enable signals synchronized to their respective clock domains. This architectural approach becomes particularly critical in system-on-chip designs containing multiple clock domains with frequency ratios that may span an order of magnitude or more, requiring careful synchronization to prevent metastability issues and ensure proper test mode transitions across all clock boundaries. The implementation of pipeline stages must balance the overhead of additional registers against the timing benefits achieved, with each stage introducing one clock cycle of latency but providing substantial improvements in signal integrity and timing margin.

The key innovation lies in the dynamic control capability introduced through test point integration, which extends beyond simple scan enable pipelining to provide fine-grained control over testing modes at the partition level. Logic gates positioned after the pipelined scan enable registers provide selective activation of the launch-on-extra-shift feature for specific portions of the design, creating a heterogeneous testing environment where different regions can operate under different launch mechanisms simultaneously or sequentially. These control points connect to specialized test point registers within scan chains, enabling runtime configuration of testing modes across different design regions through simple scan-based programming operations that require no additional test access mechanisms. As detailed in research on digital system test and testable design using hardware description language models and architectures [6], the strategic insertion of test points and control structures enables enhanced controllability and observability throughout complex digital systems. The methodology emphasizes the importance of architectural-level considerations in testable design, where control point placement decisions made during the design phase significantly impact the effectiveness and efficiency of subsequent test generation and application. This flexibility permits adaptive testing strategies that can emphasize different launch mechanisms based on circuit characteristics, timing sensitivities, and power profiles of various design partitions. For instance, timing-critical paths in high-frequency processor cores may utilize launch-off-capture testing to avoid the stringent scan enable timing requirements, while peripheral logic blocks operating at lower frequencies can employ launch-on-extra-shift testing to benefit from the pattern generation efficiency and improved transition fault coverage. The partition-based approach also enables power-aware

testing strategies where only a subset of the design remains active during any given test pattern, reducing peak power consumption during launch and capture cycles by distributing the switching activity temporally across multiple test sequences rather than spatially across the entire chip simultaneously.

Architectural Feature	Implementation Details	Benefits	Trade-offs
Pipeline Register Distribution	Strategic placement throughout the design hierarchy	Adequate setup time for downstream logic	Additional register overhead
Signal Delay Management	External to internal delayed version generation	Decouples external interface from internal timing	One clock cycle latency per stage
Clock Domain Crossing	Synchronized scan enables per clock domain	Prevents metastability issues	Requires careful synchronization logic
Frequency Ratio Handling	Support for order of magnitude differences	Enables multi-frequency SoC testing	Complex timing closure requirements
Timing Margin Improvement	Pipeline stage insertion	Substantial signal integrity enhancement	Increased design complexity
Test Mode Transitions	Synchronized across all clock boundaries	Proper mode switching in multi-domain designs	Additional validation requirements

Table 2: Pipelined Scan Enable Architecture Characteristics [5, 6]

Power Management Through Strategic Clock Gating

Managing capture state element switching activity represents the central challenge when deploying launch-on-extra-shift testing, as the inherent characteristics of this testing methodology tend to produce higher switching rates compared to traditional launch-off-capture approaches. Excessive switching during capture cycles elevates power consumption and minimum operating voltage requirements, potentially negating the coverage benefits of enhanced testing methodologies. Research on low-power scan testing methodologies [7] has demonstrated that test power consumption can significantly exceed functional power levels, creating reliability concerns and potential yield loss. The work addresses the fundamental challenge of reducing power dissipation during scan testing while maintaining high fault coverage levels. These voltage drops introduce additional propagation delays that can cause functional circuits to fail timing tests, resulting in test-induced yield loss where perfectly operational devices are incorrectly rejected during manufacturing tests. The challenge is compounded in advanced process nodes where lower supply voltages and higher clock frequencies create narrower timing margins, making designs increasingly sensitive to even modest voltage variations. The minimum operating voltage requirements can increase substantially when excessive switching activity occurs, as the power delivery network must compensate for the peak current demands during test operations. This elevation in minimum voltage requirements has direct economic implications, as it may force designs to operate at higher voltages during testing than during normal functional operation, potentially requiring specialized test equipment or creating thermal management challenges that complicate high-volume manufacturing test processes.

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The solution involves strategic insertion of control test points connected to functional clock gating cells throughout the design, creating a hierarchical power management infrastructure that can selectively activate or deactivate portions of the circuit during test operations. These test points, integrated into scan chains for accessibility, provide selective clock disabling during test operations without requiring additional test access mechanisms or external control signals beyond the standard scan interface. The connection strategy considers multiple factors: the physical placement of clock gating cells to minimize routing congestion and timing impact, the number of sequential elements driven by each gating cell to ensure balanced partitioning, and the clock distribution network topology to maintain clock tree symmetry and minimize skew. According to research on low-power testing of CMOS circuits [8], power dissipation management during test operations requires comprehensive strategies that address both dynamic switching power and the structural characteristics of test patterns. The study emphasizes that test power reduction techniques must be integrated into the design flow to be effective, as post-generation pattern modification approaches have limited impact. For designs utilizing clock mesh architectures with multiple clock source entry points, different test points control gating cells associated with distinct clock sources, ensuring balanced power distribution across the entire power delivery network and preventing localized hotspots that could trigger over-current protection mechanisms. This partitioning approach enables testing of individual design regions sequentially rather than simultaneously, reducing both launch and capture power by limiting the number of actively switching elements during any given test cycle. The method preserves pattern count and test quality while achieving power reduction through temporal and spatial separation of testing activity, effectively trading increased test time for reduced instantaneous power consumption without sacrificing the fault detection capabilities of the original test pattern set.

Challenge Category	Impact on Design	Consequence	Affected Parameter	Process Node Sensitivity
Excessive Switching Activity	Elevated power consumption	Test power exceeds functional power	Peak current demand	High in advanced nodes
Voltage Drop Effects	Additional propagation delays	Functional circuits fail timing tests	Signal timing margins	Critical at lower voltages
Test-Induced Yield Loss	False test failures	Operational devices rejected	Manufacturing yield	Increases with voltage scaling
Minimum Operating Voltage	Increased voltage requirements	Higher test voltage than functional	Power delivery network capacity	Significant in low-power designs
Timing Margin Reduction	Sensitivity to voltage variations	Reduced design robustness	Setup/hold time margins	Critical at high frequencies
Thermal Management	Heat dissipation challenges	Specialized equipment needs	Test environment complexity	High in dense designs
Economic Impact	Specialized test equipment	Increased manufacturing cost	Production economics	Universal across technologies

Table 3: Power Management Challenges in Launch-On-Extra-Shift Testing [7, 8]

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Implementation Strategy and Validation

Successful implementation requires careful analysis of switching behavior across test patterns to identify problematic scenarios before committing to physical design implementation. Simulation-based approaches generate detailed switching activity data that identifies power hotspots and high-transition capture cycles through value change dump file analysis and power estimation tools. Research on power optimization techniques during testing [9] has established comprehensive methodologies for analyzing and managing power dissipation throughout the test application process. The work addresses the critical challenge of balancing test quality requirements with power constraints, demonstrating that strategic analysis of switching patterns can reveal opportunities for power reduction without compromising fault detection capabilities. This analysis informs multiple optimization strategies during physical implementation, including targeted cell placement adjustments that distribute high-activity logic across multiple power domains, local power grid reinforcement in identified high-activity regions through additional via insertion and metal layer utilization, and strategic buffer insertion to balance signal arrival times and reduce simultaneous switching. The validation process typically involves iterative refinement where initial test pattern sets are analyzed, problematic patterns or cycles are identified through statistical analysis of switching activity distributions, physical design modifications are implemented to address identified hotspots, and the modified design is re-validated to ensure that power constraints are satisfied while maintaining timing closure. Advanced simulation methodologies can model the interaction between switching activity and power delivery network response, predicting voltage drop magnitudes and enabling confident design sign-off without requiring extensive silicon characterization. The correlation between simulation predictions and actual silicon behavior becomes critical for high-volume manufacturing, where even small percentages of test-induced yield loss translate to significant economic impact across millions of units produced.

The implementation also supports mixed testing strategies where different design sections employ different launch mechanisms based on their specific characteristics, creating a heterogeneous testing environment optimized for each region's unique requirements. Timing-critical logic or regions identified as power hotspots can utilize launch-off-capture testing, which provides more controlled switching patterns and reduced peak power at the cost of increased pattern count and generation time, while other areas benefit from the enhanced coverage of launch-on-extra-shift methods that can detect transition faults with higher efficiency. According to research on low-power test data compression based on linear feedback shift register reseeding [10], power-aware test generation and compression techniques can achieve significant reductions in test power while maintaining high fault coverage levels. The study demonstrates that reseeding-based approaches enable efficient test data delivery with reduced switching activity during pattern application, addressing both test data volume and power dissipation challenges simultaneously. This selective approach optimizes the balance between coverage objectives and power constraints across the entire design, effectively allowing each partition to operate under the testing methodology most suited to its characteristics. The partition-level optimization extends to test scheduling, where the sequence of pattern application can be organized to ensure that high-power patterns affecting different regions are temporally separated, preventing coincident peak power events that could exceed power delivery network capabilities. Implementation experience has shown that careful orchestration of mixed testing strategies can maintain overall test time within acceptable limits while achieving both coverage targets and power constraints that would be unattainable with uniform application of a single testing methodology across the entire design.

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Implementation Phase	Analysis Method	Optimization Strategy	Target Outcome	Validation Approach
Switching Behavior Analysis	Value change dump file analysis	Power hotspot identification	Problematic scenario detection	Pre-implementation simulation
Power Estimation	Power estimation tools	High-transition cycle identification	Capture cycle optimization	Statistical distribution analysis
Cell Placement Optimization	Activity distribution analysis	High-activity logic spreading	Multi-domain power distribution	Iterative refinement
Power Grid Reinforcement	Hotspot region identification	Via insertion and metal layer utilization	Local grid strengthening	Post-modification validation
Buffer Insertion Strategy	Signal timing analysis	Strategic buffer placement	Simultaneous switching reduction	Timing closure verification
Pattern Set Analysis	Statistical switching analysis	Problematic pattern identification	Pattern-level optimization	Re-validation cycle
Power Network Modeling	Advanced simulation	Switching-PDN interaction	Voltage drop prediction	Silicon correlation
Design Sign-off	Predictive modeling	Constraint satisfaction	Confident release	Pre-silicon validation

Table 4: Simulation-Based Analysis and Physical Implementation Optimization [9, 10]

Conclusion

The integration of launch-on-extra-shift architecture with strategic power management through clock gating control represents a significant advancement in at-speed testing methodology for contemporary integrated circuits. This comprehensive article successfully addresses the traditional tradeoff between test coverage and power consumption by enabling dynamic control over launch mechanisms at the partition level while implementing hierarchical power management infrastructure throughout the design. The pipelined scan enable architecture provides the foundational timing flexibility required to support mixed testing strategies, where timing-critical regions employ launch-off-capture methods while other areas benefit from the enhanced efficiency of launch-on-extra-shift testing. Strategic insertion of control test points connected to functional clock gating cells enables selective activation of design regions during test operations, achieving substantial power reduction through temporal and spatial separation of switching activity without compromising the fault detection capabilities of optimized test pattern sets. Implementation validation through simulation-based analysis and iterative physical design refinement ensures that power constraints are satisfied while maintaining timing closure and manufacturing yield targets. The article demonstrates that careful orchestration of heterogeneous testing environments, combined with power-aware design-for-testability structures integrated early in the design flow, can achieve coverage improvements while operating within stringent power envelopes necessary for high-yield, cost-effective production. This

article establishes that sophisticated architectural support, when combined with comprehensive analysis and validation processes, enables the semiconductor industry to meet the increasingly demanding requirements of advanced process nodes where timing margins continue to narrow and power delivery challenges intensify, ultimately delivering both superior test quality and acceptable manufacturing economics.

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