Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

AI-Augmented Verification for Next-Generation VLSI Systems: Challenges, Techniques and Future Directions

Suri Babu Talla

AMD, USA

ARTICLE INFO

Received: 27 Feb 2026

Accepted: 02 March 2026

ABSTRACT

The verification problems in the semiconductor industry have never been more of a challenge as the System-on-Chip architectures bring in heterogeneous computing units, sophisticated memory hierarchies and various interface standards into an ever-more complex silicon implementation. Design verification has become the most popular bottleneck in semiconductor development, consuming large amounts of engineering resources and failing to cope with the exponentially growing state-space and protocol diversity. Artificial Intelligence can provide a groundbreaking direction with the possibility to automate the verification processes with scalable, data-driven solutions. Machine learning is an effective system in the extraction of patterns within huge simulation logs, coverage databases and regression histories that go unexploited during traditional processing. Early applications such as intelligent test generation with reinforcement learning, automated debug assisting with failure clustering and waveform pattern recognition, coverage optimization with predictive analytics and natural language processing with verification planning have shown verifiable improvements in verification efficiency. The combination of advanced machine learning algorithms, convenient compute infrastructure in the cloud and the availability of extensive verification data sets places AI as a real leverage of modern verification systems as an extension layer. Nevertheless, in order to achieve full potential, it is necessary to overcome issues associated with the quality of data, interpretability of the models, integration with the existing UVM and formal verification flows and cross-design generalization. The trend is to AI-native verification ecosystems where engineers are no longer engaged in manual test development but only in managing intelligent automation processes.

Keywords: VLSI Verification, Artificial Intelligence, Machine Learning, Test Generation, Coverage Optimization

1. Introduction

The semiconductor industry is also experiencing a paradigm shift as the complexity of the integrated circuits keeps increasing beyond the reach of conventional design and verification techniques. State-of-the-art System-on- Chip architectures combine heterogeneous computing units, advanced memory architecture and high-speed interconnects that pose significant challenges to traditional verification methods. It has been proven that artificial intelligence and machine learning methods incorporated into VLSI design processes constitute a paradigm shift in the manner in which semiconductor development organizations solve complex engineering issues [1]. Design verification is now proving to be the most resource-consuming phase of the development lifecycle and in most instances, it is taking over most of the project engineering time as well as project engineering budget.[3]

Combining machine learning algorithms, scalable computing infrastructure and large datasets to verify has presented positive conditions to automation by artificial intelligence. Analysis of AI in the VLSI physical design Industry has found numerous opportunities in intelligent optimization, automatic decision making and better design exploration capabilities at various phases of the semiconductor development flow [2]. These opportunities naturally lead to functional verification, in

Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

which the exponentially expanding space of design states has made exhaustive manual testing increasingly impractical. The AI adoption motivation is a result of the understanding that the complexity of verification increases at a higher rate than design complexity directly and it faces unsustainable growth that poses significant endangering effects on development schedules and silicon yield.

The paper analyzes enabling technologies, real-world applications and implementation issues related to the application of AI in VLSI verification and offers a full-fledged framework to understand how intelligent automation can support the conventional verification methodologies, as well as tackle the scaling constraints of the conventional methods.

2. The Growing Complexity of Verification

Modern VLSI systems have become extremely complex structures incorporating numerous processing units, intelligent accelerators, sophisticated memory subsystems and a wide variety of interface protocols on a single chip implementation. This design complexity has fundamentally changed the verification problem by increasing the problem space in several dimensions that increases the overall engineering load. Multi-core processor designs need coherency protocols, inter processor communication systems and shared resource arbitration policies to be thoroughly tested. Heterogeneous accelerators such as graphics processing units, neural network inference engines and domain-specific compute elements pose specialized functional behaviors, which require focused tactics of verification. The exploration of foundation AI models in VLSI circuit design and electronic design automation has shown that the use of big language models and more advanced machine learning designs can solve complexity issues at both ends of the design and verification spectrum from RTL development to physical implementation [3].

Modern SoCs have an interface diversity attribute that leads to significant verification challenges that are beyond core functional validation. Modern designs are required to accommodate many industry-standard protocols such as PCI Express through many generations, USB standards, interfaces to memory such as DDR, LPDDR and high-speed serial connections to networking and display. The intellectual property of each interface protocol needs specific verification, protocol-aware stimulus generation and compliance checking infrastructure, which is a huge development cost. Research investigating the usage of neural networks in VLSI design and verification has reported the use of neural network structures in improving protocol verification by generating tests intelligently, conducting compliance analysis automatically and refining stimulus generation based on coverage feedback [4]. The extension of the low-power design strategies induces new verification aspects regarding power domain control, transitions in voltage scaling, retention characteristics and the operation of isolated cells that should be verified in all the working conditions.

Complexity Category	Key Elements	Verification Impact
Architectural	Multi-core processors, heterogeneous accelerators, memory hierarchies	Cache coherency validation, inter-processor communication testing
Interface Protocols	PCIe, USB, DDR/LPDDR, high-speed serial links	Protocol-aware stimulus, compliance checking
Power Management	Voltage scaling, power domains, retention logic	Low-power UPF validation, isolation verification
State Space	Combinatorial interactions, operating modes	Corner-case exploration limitations

Table 1: Verification of Complexity Dimensions [3, 4].

Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

The basic state space explosion issue restricts the usefulness of the conventional constrained-random verification strategies in spite of the available computing resources invested in simulation. Even more complex coverage-based methods often have cases of critically important corner cases that have not been covered even after many cycles of regression. The design feature, operation mode and environmental conditions all combine in a combinatorial interaction that forms verification scenarios that cannot be fully listed by manual test planning. Another major challenge is debugging activities, as engineers must find a way of correlating failure symptoms at various levels of abstraction, explore huge waveforms and intricate signal interactions. Combined, these issues have made verification the most significant bottleneck in the development programs of semiconductors, spurring an interest in AI-based automation as a possible avenue to sustainable verification scaling.

3. Why AI Is Poised to Transform Verification

The circumstances that made AI suitable in design verification have reached a high level of maturity due to the integration of algorithmic innovations, infrastructure accessibility and data unavailability. The processes of verification produce large amounts of structured and semi-structured data such as simulation logs, coverage databases, assertion reports, waveform archives, emulation results and regression histories across multiple project phases. This data has traditionally been underutilized due to the impossibility of the manual analysis methods to process the amount of information generated by the modern verification environment, its quantity, variety and speed. The field of position verification represents a perfect field of application of AI-driven automation and intelligent decision support because machine learning algorithms are effective at extracting patterns out of massive amounts of data. That integration in VLSI development Conference papers discussing the application of machine learning models have reported how machine learning models can be used to extract practical insights about verification data that would otherwise be unfeasible to detect using more traditional analysis methodologies [5].

The computing hardware needed to execute advanced AI architectures has become more available to semiconductor development groups of different sizes. Simulation platforms based on cloud offer elastic computing capabilities that can support both traditional regression workloads, as well as machine learning training and inference workloads without special purpose capital investment. Emulation systems have now developed to accommodate designs of significant complexity and performance characteristics appropriate to the production of meaningful datasets to apply AI applications. The presence of both GPU clusters and specialized accelerator hardware has lowered the costs of training more complex models on verification data. Industry attitudes towards AI have been felt across the VLSI development process, as machine learning methods can be used to streamline verification processes by forecasting verification coverage, detecting test redundancy and suggesting stimulus adjustments to enhance an overall verification process in terms of efficiency and effectiveness [6].

Enabler Category	Components	Verification Benefit
Data Abundance	Simulation logs, coverage databases, waveform archives, regression histories	Pattern extraction, predictive analytics
Compute Infrastructure	Cloud platforms, emulation systems, GPU clusters	Scalable ML training, parallel inference
ML Algorithms	Reinforcement learning, anomaly detection, NLP, graph neural networks	State exploration, specification parsing

Table 2: AI Enablers for Verification Transformation [5, 6].

Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Machine learning algorithm development has created methods that are best adapted to the structure of verification problems. The design of state space can be explored effectively using reinforcement learning structures to learn policies that put greater emphasis on test scenarios with a high value due to the feedback of cover and bug discovery. Anomaly detection algorithms detect the presence of unusual patterns of behavior in the output of the simulation and these patterns may represent the existence of subtle functional errors that elude the traditional checker mechanisms. NLP can also be used to automatically process design specification and produce verification artifacts such as assertions, coverage specifications and test intent specifications. Graph neural networks are shown to be useful in analysis of circuit structure and prediction of functional relationships used to develop verification strategies. The information maturity of these artificial intelligence methods makes AI a viable augmentation layer to verification processes as opposed to a hypothetical future feature that would involve additional investment into research.

4. Early Applications of AI in Design Verification

Artificial intelligence has already started providing quantifiable value in various areas of verification, proving that it is practically applicable and not just a matter of theory but can be implemented in production. One of the most influential early uses is the intelligent test generation, in which reinforcement learning and generative models are used to generate test scenarios that are as fully covered as possible but reveal corner-case bugs. These methods use information about historical regressions to learn state-space areas that are not over explored using traditional constrained-random stimulus to generate tests in scenarios with a high probability of revealing functional errors. Publications in journals that discuss the use of AI to produce tests in the electronics and integrated circuit design fields have reported how test generation based on machine learning is more effective at the targets of coverage than classical random techniques and that it has identified bugs that are not effectively found using traditional verification techniques [7]. The capability to keep on improving testing quality according to the results of the regression develops a feedback loop that improves the effectiveness of the verification with each project stage.

Automated debug and root-cause analysis features deal with one of the most time-intensive tasks of verification processes. The AI-driven tools examine the signatures of failure, group related bugs according to the nature of symptoms and match observed behaviors with probable root causes according to the patterns that were acquired during the historical debug experience. The pattern recognition algorithms detect the relationships in waveforms and timing anomalies, which reveal particular failure mechanisms, which are used to detect the diagnostic process faster. These studies have been published in the international journals on information technology and management, which discuss how the engineering effort needed on failures analysis in connection with the engineering effort needed to identify root-causes can be significantly reduced when intelligent debug assistance is used to examine failures [8]. The tools with AI support help to reduce the number of minutes spent on mechanical debug operations and allow the verification team to spend their time on valuable analysis work that may need human judgment, architecture knowledge and innovation to solve the problem.

Another field of high practical value in the context of production verification is coverage optimization with the help of AI. Machine learning models determine redundant tests with insignificant contribution to the coverage progress, determine gaps in coverage prediction using analysis of the design structure and suggest specific stimulus changes that effectively seal certain coverage gaps. The ability is especially useful in large SoC programs where regression infrastructure is a serious recurring cost and cycle time has a direct effect on project schedules. Predictive coverage analytics allow efficient resource allocation in deciding verification planning, eliminating wasteful redundant simulation, in competing priorities of verification.

Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

Application Domain	AI Technique	Functional Outcome
Test Generation	Reinforcement learning, generative models	Coverage maximization, corner-case discovery
Debug Automation	Failure clustering, waveform pattern recognition	Root-cause identification, symptom correlation
Coverage Optimization	Predictive analytics, redundancy detection	Gap closure, resource allocation
Anomaly Detection	Outlier identification, deviation flagging	Subtle bug discovery
Verification Planning	Natural language processing	Assertion generation, requirement extraction

Table 3: AI Applications in Verification [7, 8].

Aberrant and outlier detection also offers an extra verification of intelligence level in detecting odd behavioral patterns that can harbor an insidious bug that a standard assertion-based checker might have overlooked. The deviations in the simulation logs, emulation traces, or performance metrics that are to be investigated are flagged by machine learning models trained on the normal operation characteristics. Verification planning activities are starting to be automated by using natural language processing applications, which interpret design specifications, derive verification requirements and produce an initial test plan or assertion template that minimizes hand effort and maximizes conformance between what was written in design and what was written in verification.

5. Challenges and Limitations of AI Adoption

In spite of strong evidence of AI usefulness in the verification processes, there are major limitations crippling extensive application and reducing the applicability of the existing applications in manufacturing settings. Quality and labelling are also the inherent barriers since machine learning models require clean and structured data that reflects the domain of verification under verification. The legacy of verification environments usually generates logs and reports having different formats that need a lot of preprocessing before being consumed by AI systems. Supervised learning and the ground truth labelling required when using ground truth are expensive and expert-only tasks, which cannot be easily or economically expanded to all verification scenarios. Papers on conference proceedings discussing the use of machine learning in the VLSI development have highlighted the fact that data preparation and curation can be expensive in terms of engineering just like the development of the AI models [9]. The fact that EDA tools do not use standardized data formats is also a problem that makes it difficult to develop generalizable AI solutions that can be transferred to various design settings.

The interpretability issues inherent in models pose a trust barrier that prevents use in engineering forms of functional correctness where any error has a significant cost impact on the silicon. Before acting upon AI suggestions, verification engineers need to know and verify these suggestions but most machine learning models are black box models that simply give outputs without a clear description of the reasoning or confidence measure behind them. The complexity of creating models, their deployment and maintenance is further complicated by the need to explainable AI practices that would give a clear rationale of why recommendations should be given. Extensive surveys of VLSI design to artificial intelligence and machine learning applications have reported interpretability

Journal of Information Systems Engineering and Management
2026, 11(2s)
e-ISSN: 2468-4376
https://www.jisem-journal.com/

Research Article

properties to be especially acute in verification settings such as false negatives in the form of missed bugs, escaped bugs and expensive silicon respins [10].

Challenge Area	Core Issue	Mitigation Requirement
Data Quality	Inconsistent formats, labeling overhead	Preprocessing pipelines, annotation frameworks
Interpretability	Black-box outputs, trust barriers	Explainable AI approaches
Flow Integration	Legacy UVM, emulation compatibility	Non-disruptive deployment
Skills Gap	Data science expertise requirements	Engineer training programs
Generalization	Design-specific model limitations	Transfer learning, retraining strategies

Table 4: AI Adoption Challenges [9, 10].

The combination with the current verification processes poses the practical implementation issues that impact the timelines of the AI adoption and the ROI. UVM-based environments, emulation environments, formal verification tools and coverage infrastructure are significant organizational investments that development teams are unwilling to interfere with or to change. AI solutions cannot be used to wholesale change the methodology but can be applied to specific processes to enhance results without posing a risk and overloading retraining. Lack of skills among verification teams is another obstacle in place, since engineers should understand the concept of data science and machine learning in order to apply AI tools and interpret their results in the right way. The generalization problem restricts the transferability of AI models to different design architectures with models that have been trained to work with particular IP families or SoC architectures potentially needing many retraining or adaptations to fit another context of verification. Such constraints highlight the idea that AI is not replacing traditional verification methodologies in real-life practice but supplementing them and that hybrid workflows, which involve AI capabilities and human expertise and engineering judgment, need to be implemented.

6. Future Directions

The future of AI in design checking is toward more complex integration and a wider area of application with the development of technologies and the experience of using it. AI-native verification as simulation and emulation tool vendors directly adds machine learning features to their products, they will offer the ability to access intelligent automation without effort or expert knowledge of AI. Autonomous test generation engines which are autoregulated to keep learning about regression results will require less manual intervention in stimulus development and more effective corner-case exploration. Predictive models that can be used to predict the bug-prone areas prior to the implementation of the RTL will facilitate the proactive allocation of verification resources according to design risk evaluation, instead of responding to found bugs.

Formal verification can be significantly helped by AI in the synthesis of properties and advice on Proofs. The design specifications and historical libraries of assertions could be analysed using machine learning techniques to suggest formal properties with high verification value, in comparison to implementation effort. AI-aided proof techniques may lead formal engines to successful convergence on properties of complexity that are not easily explored by exhaustive state space

exploration. Reinforcement learning is also integrated with formal methods and this leads to the opportunities of integrating hybrid approaches that can combine the advantages of both paradigms without furthering the limitations each has.

Pipelines of machine learning, large-scale data analytics and cloud-based verification will become end-to-end as organizations develop their AI adoption strategies and build operational experience of intelligent verification pipelines. Such combined environments will facilitate learning that is sustained by verification results and verification intelligence can become better over time through program lifecycles and across successive generations of products. Verification engineers will stop their manual test generation and debugging of failures and move to overseeing AI-based processes, checking model results and attention to architectural correctness and system-level behavior that needs human judgment and expertise.

Conclusion

The growing complexity of recent VLSI systems has defined design verification as a serious bottleneck limiting the efficiency of semiconductor development and silicon success rates. Although mature and highly developed over decades of experience in the industry, traditional verification methodologies are inherently limited in terms of the exponential growth of state-space, protocol diversity and safety issues that modern SoC designs present. The semiconductor industry has evolved where a slight enhancement to the existing strategies is not enough to sustain the effectiveness of verifications in the competitive development cycles. AI also brings about scalable and data-driven automation that augments and complements human expertise throughout verification processes. The application of intelligent test generation, automated debug support, coverage optimization, anomaly detection and verification planning based on NLP indicates that AI has a positive impact on conventional methods and provides verification efficiency advantages. The combination of self-learned machine learning algorithms, available compute resources and large verification datasets mean that AI is more of an extension of the recent verification cultures and not a radical overthrow. The way to go is hybrid workflows with AI capacity and the application of domain knowledge plus engineering judgment in verification teams. With becoming mature tools, the industry will evolve to AI-based verification ecosystems that will shift the task of verification engineers from developing manual tests to intelligent workflow monitoring and ensuring architectural correctness.

References

[1] Janaki Rama Phanendra Kumar Ande and Md Abul Khair, "High-Performance VLSI Architectures for Artificial Intelligence and Machine Learning Applications," HAL Open Science, 2019. [Online]. Available: https://hal.science/hal-04525631/document

[2] Japesh Kumar, "AI in VLSI Physical Design: Opportunities and Challenges," 2025. [Online]. Available: https://www.design-reuse.com/article/61623-ai-in-vlsi-physical-design-opportunities-and-challenges/

[3] Ram Mohan Reddy Kundavaram, Rahul Reddy Bandhela, Abhishake Reddy Onteddu. (2022). AI-Driven Predictive Modeling In Healthcare: A Data Science Perspective On U.S. Healthcare Data. South Eastern European Journal of Public Health. https://doi.org/10.70135/seejph.vi.6691

[4] Wenji Fang et al., "A Survey of Circuit Foundation Model: Foundation AI Models for VLSI Circuit Design and EDA," arXiv:2504.03711, 2025. [Online]. Available: https://arxiv.org/abs/2504.03711

[5] Diana Dranga and Catalin Dumitrescu, "Artificial Intelligence Application in the Field of Functional Verification," MDPI, 2024. [Online]. Available: https://www.mdpi.com/2079-9292/13/12/2361

[6] Nisha Milind Shrirao, "Intelligent Design Automation in VLSI Systems: Leveraging AI for Future Electronics Applications," SCCTS, 2024. [Online]. Available: https://eccsubmit.com/index.php/congress/article/view/48
[7] Prasanth S., "How can AI impact the VLSI development cycle and what are such AI enabled EDA tools?," LinkedIn, 2023. [Online]. Available: https://www.linkedin.com/pulse/how-can-ai-impact-vlsi-development-cycle-what-enabled-sathyamoorthy/
[8] Haijian Zhang et al., "Physics-Informed Neural Networks for High-Fidelity Electromagnetic Field Approximation in VLSI and RF EDA Applications," JCEIM, 2025. [Online]. Available: https://jceim.org/index.php/ojs/article/view/100
[9] Yuvaraj J Patil, "Artificial Intelligence In Functional Verification: Transforming Safetycritical Semiconductor Design Methodologies," IJITMIS, 2025. [Online]. Available: https://iaeme.com/MasterAdmin/Journal_uploads/IJITMIS/VOLUME_16_ISSUE_2/IJITMIS_16_02_059.pdf
[10] Laith Ahmed Najam and Rebert H. Luedkea, "AI-Enhanced Design Automation for Next-Gen Electronics Applications and VLSI Systems," SCCTS, 2024. [Online]. Available: https://eccsubmit.com/index.php/congress/article/view/19
[11] Arun Sadanand Tigadi, "Survey On VLSI Design For Artificial Intelligence And Machine Learning Applications," ResearchGate, 2023. [Online]. Available: https://www.researchgate.net/publication/370519687_Survey_On_VLSI_Design_For_Artificial_Intelligence_And_Machine_Learning_Applications