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Research Article

Optimal THD Reduction in Multilevel Inverters Using PID and Fuzzy Logic Control

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ABSTRACT

Multilevel inverters (MLIs) are becoming essential for most high-voltage, high-power, and medium-voltage electronic applications. MLIs offer a range of output levels suitable for satisfying the varied demands of high-voltage and power applications. Besides enhancing output levels, MLI can reduce voltage stress (dv/dt) and the total harmonic distortion across the power switches. The extensive advancement of new MLI topologies on current ones enhances the ability to increase output levels while utilizing fewer components. Three significant topologies of multilevel inverters are compared in this work: cascaded H-bridge inverters, diode-clamped inverters, and flying capacitors. Electromagnetic interference (EMI) and total harmonic distortion results are compared. To do this comparison, meticulous MATLAB/Simulink simulations are used to analyze these inverters. Three configurations of inverters are simulated. There are three types of phases: single-phase, three-level, and five-level. Based on the comprehensive MATLAB/Simulink simulation results, a comparison of the efficacy of these multilevel inverters is possible. Alongside conducting a comparative analysis of established topologies, Traditional multilevel inverter designs frequently encounter complexity issues, highlighting the need for a more simplified approach. This study introduces a novel structure known as the 'packed u-cell 5 ' within the MATLAB/Simulink software. Its THD characteristics are analyzed to assess the efficacy of this novel structure. By implementing PID control, the work also seeks to enhance the total harmonic distortion performance of the 'packed u-cell 5 ' structure. After that, we used a Fuzzy Logic Controller (FLC) with a Mamdani type. Simulation results show that the PUC inverter with the Fuzzy Logic Control successfully maintains the output voltage level within the desired range. Furthermore, to assess the superiority of the Fuzzy Logic Control, a comparative evaluation is conducted between the Fuzzy Logic Control and PID Control methods for the packed U-Cell 5 inverter. The results reveal that the FLC exhibits more consistent and reliable feedback compared to the PID controller. A comparative analysis of their total harmonic distortion and electromagnetic interference outputs was conducted via simulations in MATLAB/Simulink.

Keywords: electromagnetic interference, Proportional-Integral-Derivative control, total harmonic distortion, PUC inverter, Fuzzy logic control.

INTRODUCTION

The world around us has evolved and expanded over the years, offering us valuable lessons. These lessons have given us the knowledge and skills to deal with the problems of an expanding population and limited energy resources. With the increasing need for energy and the harmful effects of the adverse impact on the world caused by regular sources, there has been a profound change in how we think about getting and using energy [1].

Photovoltaic (PV) technology represents a promising form of renewable energy. The capacity and usage of PV installations are increasing every day [2,3]. The converter utilised in the photovoltaic system is essential for transporting electricity from the photovoltaic source to the

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consumer, utility, and grid. The PV converter can be classified based on the galvanic isolation operation.[1] Multilevel converters, in particular, provide substantial advantages regarding enhanced power quality and fewer harmonics. Various modules exist for multilevel inverters, including the Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascade H-Bridge (CHB) modules.[2].

Previous research has investigated many MLI topologies, such as cascaded H-bridge, diode-clamped, and flying capacitor inverters. Although these systems have shown significant benefits in minimizing THD, optimizing their performance using advanced control techniques, like PID and fuzzy logic, continues to pose a problem. Furthermore, the advancement of innovative inverter architectures that reduce complexity while enhancing efficiency is a subject of ongoing investigation.

Including selective harmonic elimination, carrier-based methods, and space vector modulation. The multicarrier-based Pulse Width Modulation (PWM) is the most prevalent control method, known for its effectiveness and simplicity in minimizing total harmonic distortion in the output voltage. Carrier-based PWM typically employs a triangular carrier waveform due to its superior harmonic performance in multi-level inverter outputs. The control of multilevel inverters is primarily accomplished using Level-shift multicarrier-based PWM techniques, such as Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), and Phase Displacement (PD). These methods are crucial for optimizing efficiency, controlling complexity, and Voltage Quality [4]. Table 1 provides a summary of the PWM techniques, highlighting aspects such as Control Complexity, efficiency, and voltage quality [5].

Table 1. provides a summary of the PWM techniques

PWM Technique	Control Complexity	Efficiency	Voltage Quality
Phase Displacement	Low to moderate complexity, making it more straightforward to implement and manage.	Typically efficient because of its more straightforward modulation strategy.	This makes it ideal for applications that demand high-quality output. Reduced Total Harmonic Distortion, combined with Good voltage quality,
Alternative Phase Opposition Disposition	The system focuses on different harmonic characteristics. But it has moderate complexity.	Efficiency, similar to POD, varies based on the targeted harmonics	Similar to POD, it targets different harmonics, improving the quality of varied voltages.
Phase Opposition Disposition	The system needs to invert alternate carrier waves. Exhibits moderate complexity, similar to APOD.	Efficiency is generally good, although it is slightly lower than PD due to the complexity of the waveforms.	Effective in improving voltage quality and reducing specific lower-order harmonics.

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OBJECTIVES

The Flying Capacitor, Neutral Point Clamped, and Cascade H-Bridge modules are among the numerous modules available for multilevel inverters. As the voltage levels increase, these structures become increasingly costly and challenging to execute.[6], The Packed U-Cell multilevel inverter has been introduced to address these challenges. The PUC inverter offers similar benefits but with fewer components compared to other topologies. It effectively achieves high voltage conversion with low harmonic distortion without a transformer.[7]. Various techniques have been developed to control PUC inverters, including the PUC5 inverter, which achieves capacitor voltage balance without needing a feedback loop. This is crucial because multilevel inverters require balanced capacitor voltages to operate correctly. Ongoing research focuses on developing accurate models and control strategies to ensure the efficient and reliable operation of the PUC multilevel converter, offering a more cost-effective and simplified solution than other topologies. The proposed methods for the PUC5 inverter aim to maintain balanced capacitor voltages without relying on a feedback loop. Simulating this inverter reveals a significant reduction in Total Harmonic Distortion (THD).

METHODS

1-Flying Capacitor Multilevel Inverter

An advanced form of power electronic converter is the Flying Capacitor Multilevel Inverter that emerged in the early 1990s, pioneered explicitly by Maynard and Foch in 1992 [8]. This inverter technology is distinguished by its use of multiple capacitors that are selectively connected and disconnected by switches to produce several discrete voltage levels. This makes it easier to change direct current into high-quality alternating current. The flying capacitor multilevel inverter is based on a modular architecture, wherein capacitors are charged to different voltage levels, acting as "flying" energy storage elements. These capacitors are then strategically switched into the circuit to synthesise varying voltage output levels. This method allows for a closer approximation of a sinusoidal waveform than traditional two-level inverters, thereby improving the overall power quality and reducing harmonic distortion. Figure 1 illustrates the circuit structure of a flying capacitor Three-phase three-level [9].

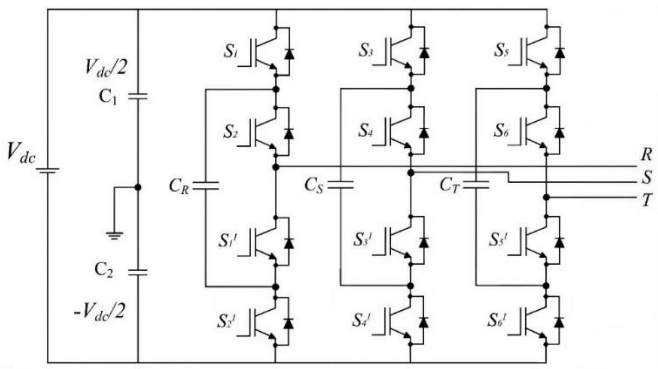

Fig. 1. Structure of multilevel flying capacitor Three-phase three-level

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Figure 2 illustrates flying capacitor's five-level, three-phase circuit structure [9].

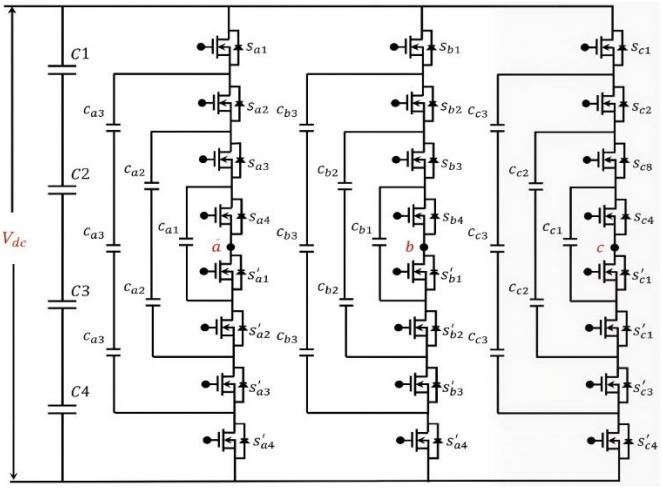

Fig. 2. Structure of multilevel flying capacitor Three-phase five-level

For $V_{an} = V_{dc} / 2$ (1)

turn on $S_{a1}, S_{a2}, S_{a3}, S_{a4}$.

For $V_{an} = V_{dc} / 4$ (2)

$a) S_{a1}, S_{a2}, S_{a3}, S'_{a1} (V_{an} = V_{dc} / 2$ of the upper $C'_4 s - V_{dc} / 4$ of $C_1)$;
$b) S_{a2}, S_{a3}, S_{a4}, S'_{a1} (V_{an} = 3V_{dc} / 4$ of $C_3 s - V_{dc} / 2$ of lower $C'_4 s)$;
$c) S_{a1}, S_{a3}, S_{a4}, S'_{a2} (V_{an} = V_{dc} / 4$ of $C_3 - V_{dc} / 2$ of $C_1 - V_{dc} / 2$ of lower $C'_4 s)$;

For $V_{an} = 0$ (3)

$a) S_{a1}, S_{a2}, S_{a3}, S'_{a1} (V_{an} = V_{dc} / 2$ of the upper $C'_4 s - V_{dc} / 4$ of $C_1)$;
$b) S_{a3}, S_{a4}, S'_{a3}, S'_{a4} (V_{an} = V_{dc} / 2$ of the upper $C_2 - V_{dc} / 2$ of $C_4)$;
$c) S_{a1}, S_{a3}, S'_{a1}, S'_{a3} (V_{an} = V_{dc} / 2$ of the upper $C'_4 s - 3V_{dc} / 4$ of $C'_3 s + V_{dc} / 2$ of $C'_2 s - V_{dc} / 4$ of $C_1)$;
$d) S_{a1}, S_{a4}, S'_{a2}, S'_{a3} (V_{an} = V_{dc} / 2$ of the upper $C'_3 s + V_{dc} / 4$ of $C_1)$;
$e) S_{a2}, S_{a4}, S'_{a2}, S'_{a4} (V_{an} = 3V_{dc} / 4$ of $C'_3 s - V_{dc} / 2$ of $C'_2 s + V_{dc} / 4$ of $C_1 - V_{dc} / 2$ of lower $C'_4 s)$;
$f) S_{a2}, S_{a3}, S'_{a1}, S'_{a4} (V_{an} = 3V_{dc} / 4$ of $C'_3 s - V_{dc} / 4$ of $C_1 + V_{dc} / 2$ of lower $C'_4 s)$;

For $V_{an} = -V_{dc} / 4$ (4)

$a) S_{a1}, S'_{a1}, S'_{a2}, S'_{a3} (V_{an} = V_{dc} / 2$ of the upper $C'_4 s - 3V_{dc} / 4$ of $C'_3 s)$;
$b) S_{a4}, S'_{a2}, S'_{a3}, S'_{a4} (V_{an} = V_{dc} / 4$ of $C_1 - V_{dc} / 2$ of lower $C'_4 s)$;
$c) S_{a3}, S'_{a1}, S'_{a3}, S'_{a4} (V_{an} = V_{dc} / 2$ of $C'_2 s - V_{dc} / 4$ of $C_1 - V_{dc} / 2$ of lower $C'_4 s)$;

For $V_{an} = -V_{dc} / 2$ (5)

turn on $S'_{a1}, S'_{a2}, S'_{a3}, S'_{a4}$.

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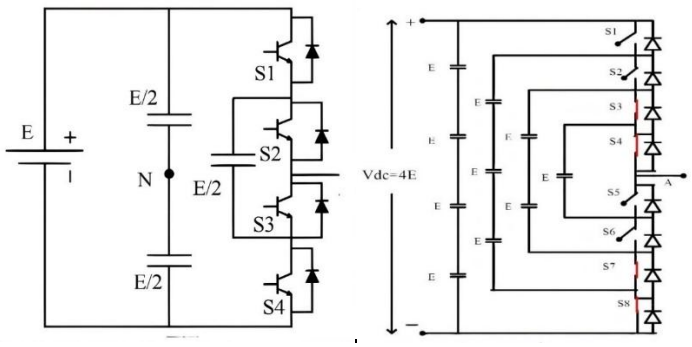

(1) (2)

Fig. 3. Flying capacitor single-phase Structures of (1) the three and (2) five levels.

Table 2 presents the five-level output voltage for the flying capacitor inverter.

Table 2. The flying capacitor inverter switching states [10].

	S1	S2	S3	S4	S5	S6	S7	S8	Voltage Output
State 1	1	1	1	1	0	0	0	0	4E
State 2	0	1	1	1	0	0	0	1	3E
Stare 3	0	0	1	1	0	0	1	1	2E
State 4	0	0	0	1	0	1	1	1	E
State 5	1	1	1	0	1	0	0	0	-E
State 6	1	1	0	0	1	1	0	0	-2E
State 7	1	1	1	0	1	1	1	1	-3E
State 8	0	0	0	0	1	1	1	1	-4E

2- Cascaded H-Bridge multilevel Inverter

This system is composed of several stages, each functioning as an independent H-bridge inverter connected to its dedicated DC power source. Each stage contains four switching devices, typically S1, S2, S3, and S4, which work together to generate various output voltages. By controlling these switches, each stage can produce output voltages of +Vdc, 0, or -Vdc. The combined output is created by adding the contributions from each stage, and the switching sequence defines the amplitude and polarity of the output. This structure allows for a flexible and modular approach to producing stepped voltage waveforms [11].

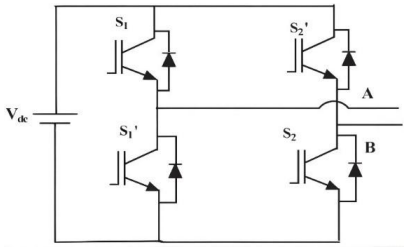

Fig. 4. Cascaded H-bridge inverter Three-level one arm [12].

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These are the voltage outputs for each switch configuration:

If all switches are turned off, the output voltage is 0.

if S4 and S2 are off and S3 and S1 are on, the output is plus Vdc.

if S4 and S2 are off and S3 and S1 are off, the output is minus Vdc.

The cascaded H-bridge inverter creates multiple voltage levels by controlling the activation of switches in each stage. The voltage increments are directly related to the level number.

A cascaded H-bridge with sources will produce discrete levels of output voltage.

$$K = (H-1)/2 \quad (6)$$

$$H = 2k+1 \quad (7)$$

$$N = m \times 2 - 2 \quad (8)$$

$$\max voltage = K \times V_{dc} \quad (9)$$

K: bridges number.
H: number of output voltage levels
N: count of switching devices.

Figure 5 illustrates the circuit structure of the five-level cascaded h bridge

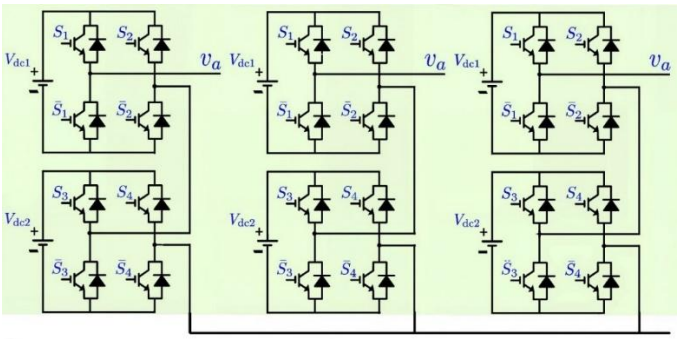

Fig. 5. Cascaded h bridge five level three phase [13].

Table 3 shows the switching states for the cascaded h-bridge.

Table 3. Switching state for the five-level cascaded h bridge

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
2 V_{dc}	on	off	off	on	on	off	off	on
V_{dc}	on	off	off	on	off	off	on	on
0	off	off	off	off	off	off	off	off
$-V_{dc}$	off	on	on	off	off	off	on	on
$-2\ V_{dc}$	off	on	on	off	off	on	on	off

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3. Diode Clamped Multilevel Inverter.

This system represents a significant advancement in inverter technology, offering improved power quality and efficiency in converting DC (direct current) to AC (alternating current). This specific type of inverter is very appropriate for high-power applications. The output waveform quality is crucial, such as in medium to high voltage levels in industrial drives, grid-connected systems for renewable energy, and electric vehicle propulsion systems [9].

A diode-clamped inverter combines multiple voltage levels to produce a stepped waveform. We link the inverter switches to a parallel circuit comprising diodes and capacitors [14]. The block diagram of the three-level Diode Clamped multilevel inverter is depicted in Figure 6.

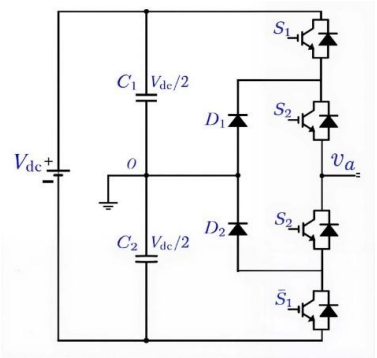

Fig. 6. Three-level diode clamped multilevel inverter

Figure 7 represents The neutral point clamped three-level, three-phase block diagram.

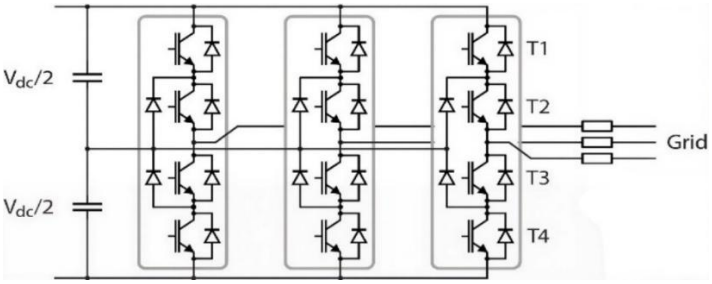

Fig. 7. NPC three-level three phase

Table 4 shows the converter's output voltage and switching pattern by phase.

Table 4. Output voltage and switching pattern produced by the converter.

	Switch Code				Output Voltage
	S_1	S_2	S_3	S_4	v_N
Switching State	On	On	Off	Off	E_d
	Off	On	On	Off	0
	Off	Off	On	On	$-E_d$

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In a 3-level diode-clamped inverter, the maximum voltage that any semiconductor switch must block is typically limited to 50% of the DC source voltage. This limitation is due to the circuit topology, where diodes are used to clamp the voltage and protect the switches. Each inverter level introduces a clamping point, which divides the total DC bus voltage among the various switches and diodes, effectively reducing the voltage stress on each component [15].

Figure 8 shows the block diagram of five level three phases of the neutral point clamped.

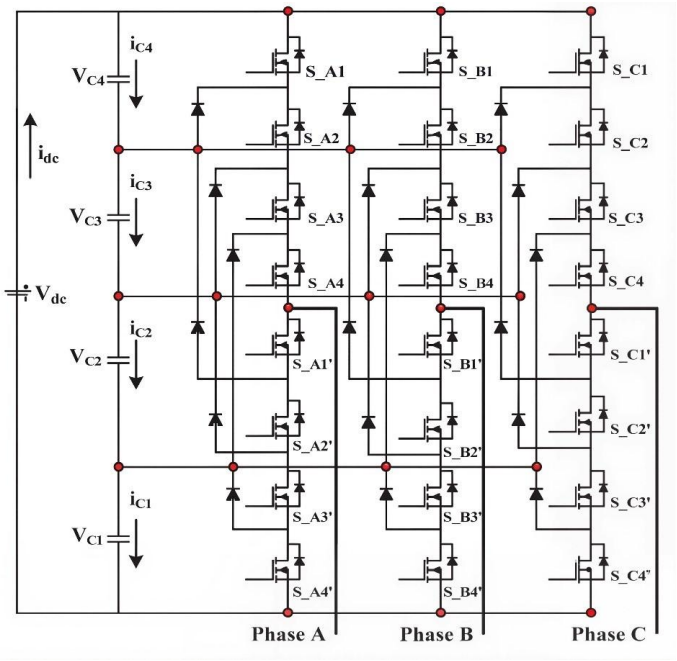

Fig. 8. A Five-Level three-phase NPC structure [12].

Assume a basic diode-clamped configuration for a phase with the following potential outputs: $+Vdc$, $+1/2Vdc$, 0, $-1/2Vdc$, and $-Vdc$. The switches can be operated as follows:

For $\boldsymbol{+Vdc}$: Activate the switches that connect the output to the positive terminal of the DC link.

For$\boldsymbol{+Vdc/2}$: Connect the output to the midpoint between the neutral and the positive terminal of the DC link.

For **0 (Neutral)**: Connect the output to the neutral point, effectively disconnecting it from both the positive and negative terminals.

For $\boldsymbol{-Vdc/2}$: Connect the output to the midpoint between the neutral and the negative terminal of the DC link.

For $\boldsymbol{-Vdc}$: Activate the switches that connect the output to the negative terminal of the DC link.

4- Packed U-cell multilevel inverter

Figure 9 illustrates the block diagram of the PUC5 inverter.

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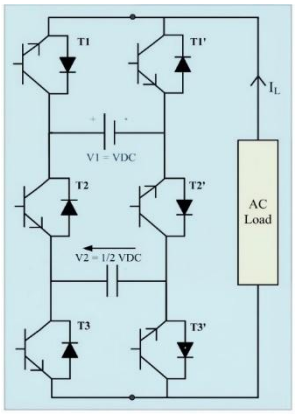

Fig. 9. PUC 5 inverter circuit [16].

The following table shows us the switching states of the PUC inverters.

Table 5. Output Voltage Levels Produced by Packed u-cell inverter [17]

	S1	S2	S3	Output
State 1	1	0	0	V1
State 2	1	0	1	V1-V2
State 3	1	1	0	V2
State 4	1	1	1	0
State 5	0	0	0	0
State 6	0	0	1	-V2
State 7	0	1	0	V2 – V1
State 8	0	1	1	-V1

The packed U-cell inverter is designed with cascaded units comprising a single switch and a DC voltage source. This structure is distinct from traditional MLIs, which typically require multiple switches and capacitors per level. The basic unit of the PUC inverter is the U cell, named for its U-shaped configuration of switches and capacitors. The PUC inverter synthesizes a desired AC output voltage by appropriately switching its U cells, which are connected in series. Each U cell can produce three voltage levels: positive, zero, and negative. By combining the outputs of multiple U cells, the PUC inverter can generate a multilevel output with reduced harmonic content. [18].

The PUC inverter is suitable for a wide range of applications, including:
Electric Vehicles (EVs): PUC inverters are employed in EVs to convert power between the battery and the motor efficiently.
Industrial Drives are utilized in variable speed drives and motor control systems to enhance performance and efficiency.
Renewable Energy Systems: It is used in photovoltaic (PV) systems and wind turbines to convert direct current power from renewable sources into alternating current power for grid integration.

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Grid-Tied Inverters: The PUC inverter is used in grid-tied applications for efficient power delivery and improved power quality.

Finally, in order to produce a waveform with multiple voltage levels, the circuit design utilizes capacitors. Its low total harmonic distortion, reduced component count, Its cost-effective design makes it well-suited for a variety of power electronic applications. [17].

Figure 10 illustrates eight possible configurations for the packed U-cell inverter.

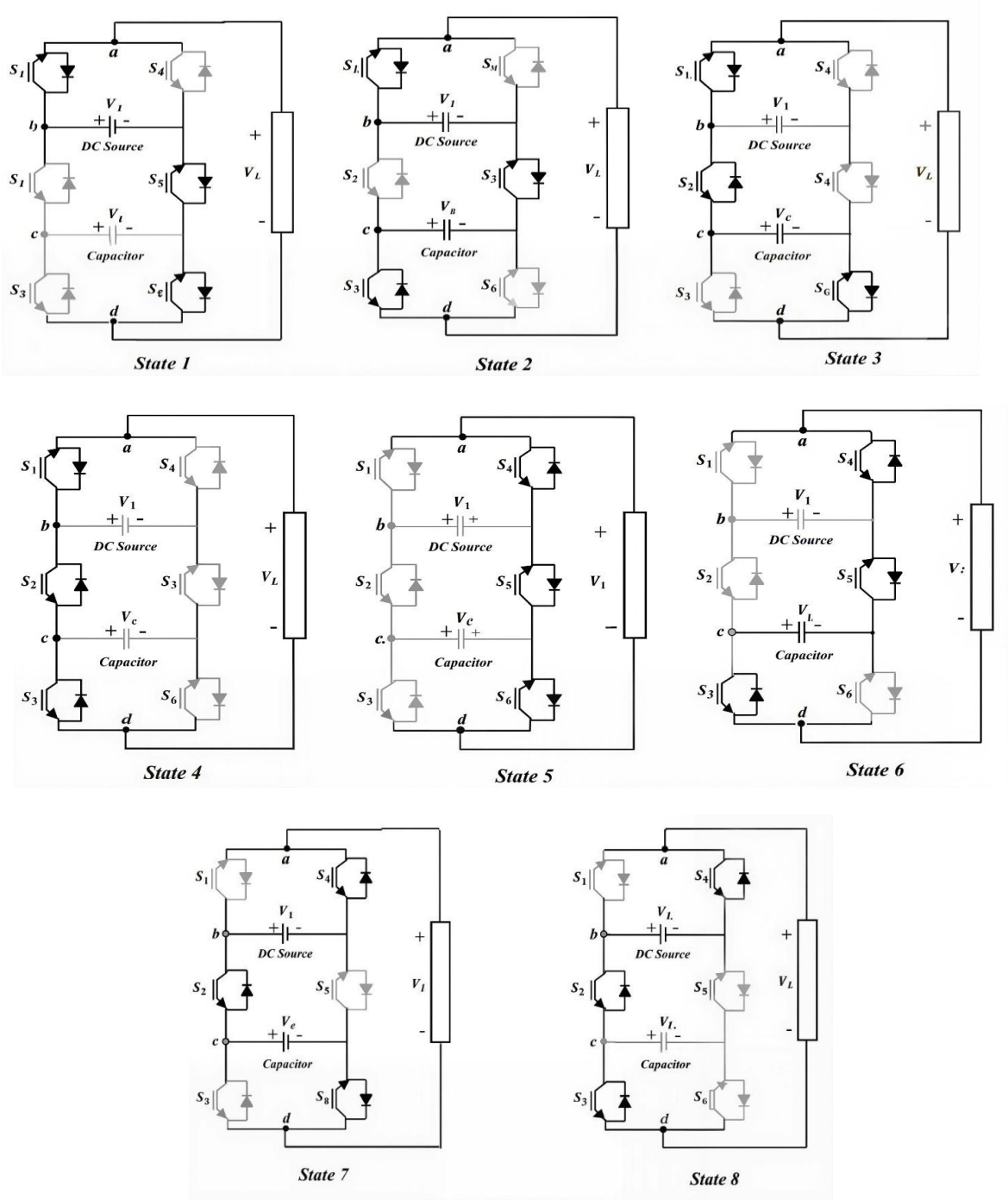

Fig. 10. Switching states through the implementation of paths [16][19].

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The five-level PUC inverter operates with only six switch states, bypassing two during each cycle [7]. The remaining switch states will be:

Switch state 1: positive charge cycle

Switch state 2: positive discharge cycle

Switch state 4: negative charge cycle

Switch state 5: negative discharge cycle

Switch state 6: Zero voltage state (neutral)

By eliminating two switching states per cycle and supplying the requisite voltage levels, the five-level PUC inverter reduces complexity and the number of switching operations. This method simplifies the control strategy, minimizes switching losses, and maintains inverter performance. [18].

The following table shows the packed U-cell connection and capacitor voltage.

Table 6. Voltage and connection of capacitors [4].

	Connected to DC supply	Connected to load	Capacitor voltage
State 1	NO	NO	No effect
State 2	YES	YES	Charging
State 3	NO	YES	Discharging
State 4	NO	NO	No effect
State 5	NO	NO	No effect
State 6	NO	YES	Discharging
State 7	YES	YES	Charging
State 8	YES	NO	No effect

A Packed U-Cell single-phase inverter setup includes two DC links and six semiconductor switches. These switches are arranged in three pairs. Four switches are connected through a DC link to form a U-cell; the complete Packed U-cell inverter comprises these U-cells. A DC supply powers the upper DC link, while the lower DC link is connected to a DC capacitor, whose voltage is regulated by a specific switching method. The voltage across the capacitor can be precisely controlled by correctly toggling the semiconductor switches. The upper two switches have double the rating of the lower four due to their exposure to higher voltage stress. This difference is because the upper switches handle the full DC supply voltage. In contrast, the lower switches are connected to the capacitor voltage, which only subjects them to half the DC supply voltage. The PUC inverter converts DC input into a high-frequency AC output. The parallel operation of the switches ensures the generation of an AC output, making the inverter suitable for various applications. The control scheme and modulation techniques are essential for producing the

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desired current and output voltage characteristics, ensuring the smooth and reliable operation of the switches and the overall system [17].

Figure 12 illustrates a proposed algorithm for the PUC 5 inverter.

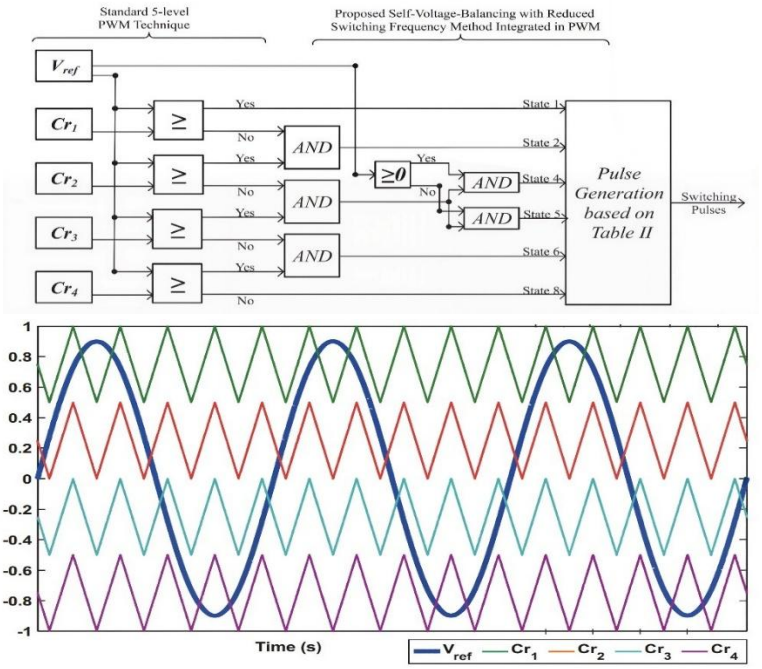

Fig. 11. A proposed algorithm for Packed U-Cell 5 inverter [20].

RESULTS

Multilevel inverters are simulated using MATLAB/Simulink to verify PWM's performance.

Table 7. Parameters of simulation for FC, NPC, and CHB multilevel inverters

parameters	value
Flying Capacitor	1/3e-6 F
Resistance	10 Ω
DC-link-voltage	100 V

Table 8. Simulation parameters for PUC5 inverter

parameters	value
Kp	0.21444
Kd	0.07058
Ki	0.15779
L	250e-3 H
DC-link-voltage	100 V
R	0.1 KΩ
C	3500e-6 F

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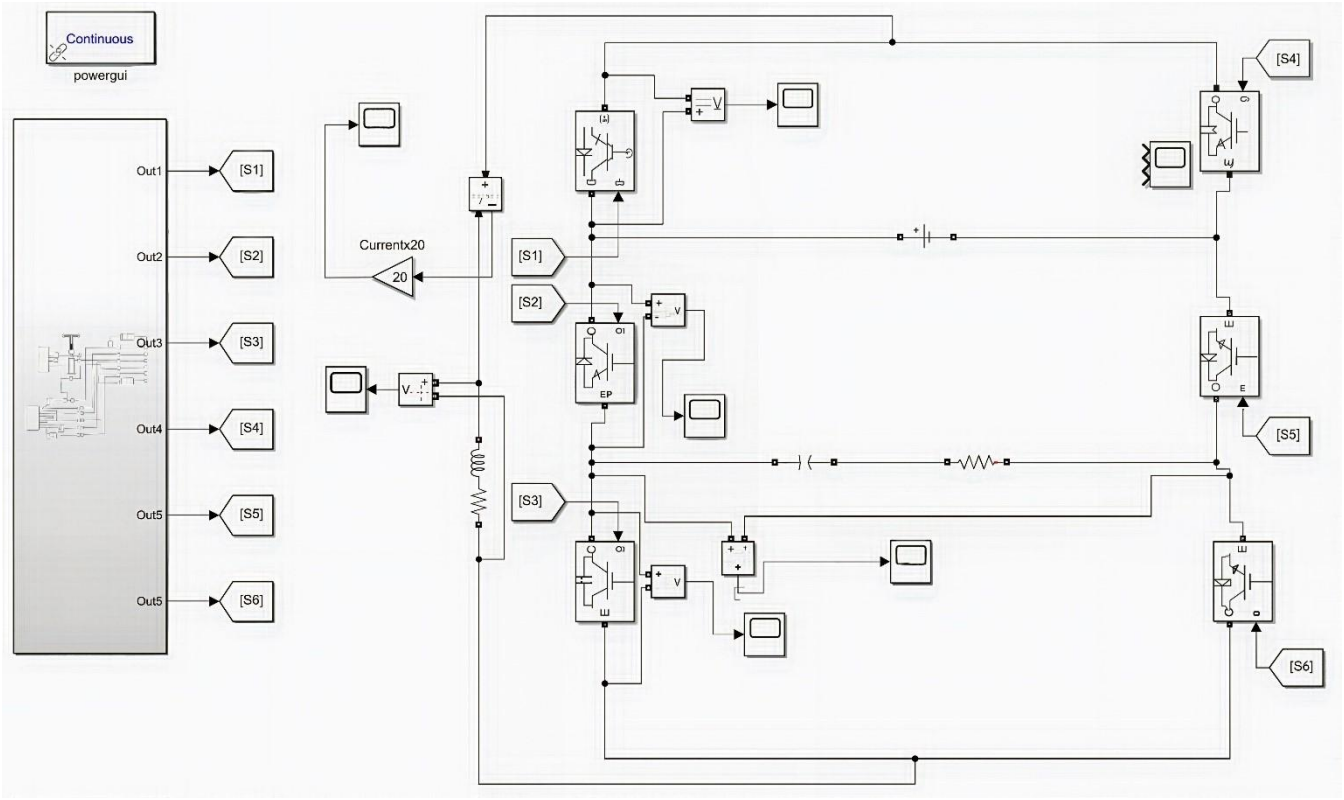
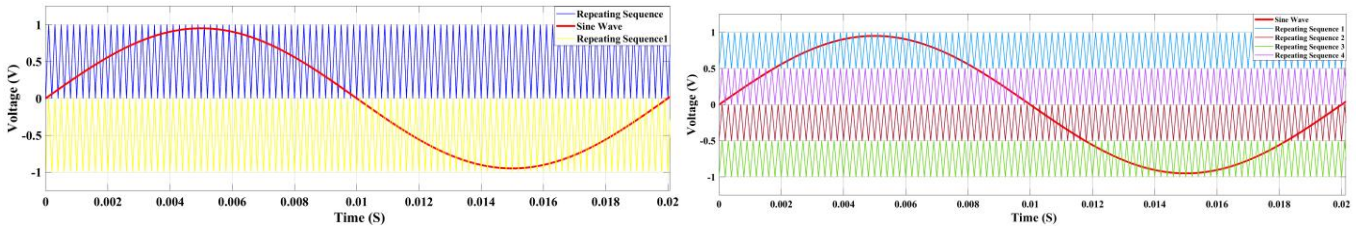


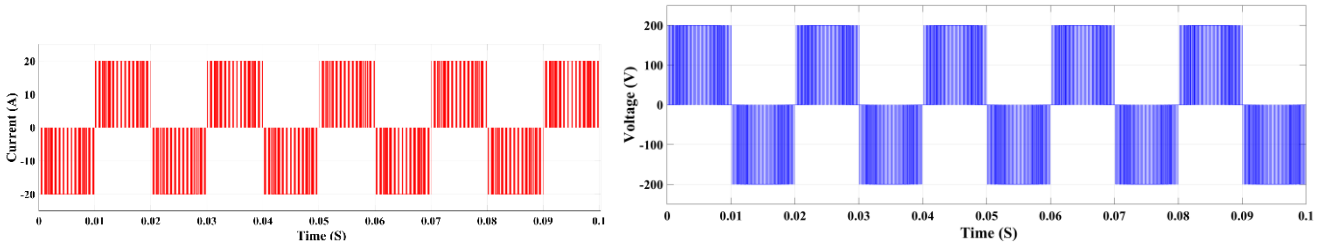
Fig. 12. PUC 5 inverter model.

The three-level and five-level topologies of the diode-clamped inverter are illustrated in Figure 13 utilizing SPWM.



(1) (2)

Fig. 13 SPWM of the diode-clamped five-level topology (1) three-level (2) five-level



(1) (2)

Fig. 14. Output current and voltage of the neutral point clamped three-level topology.

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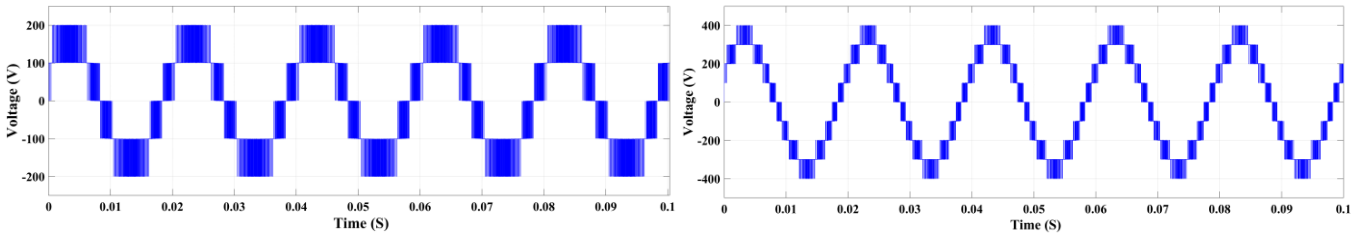
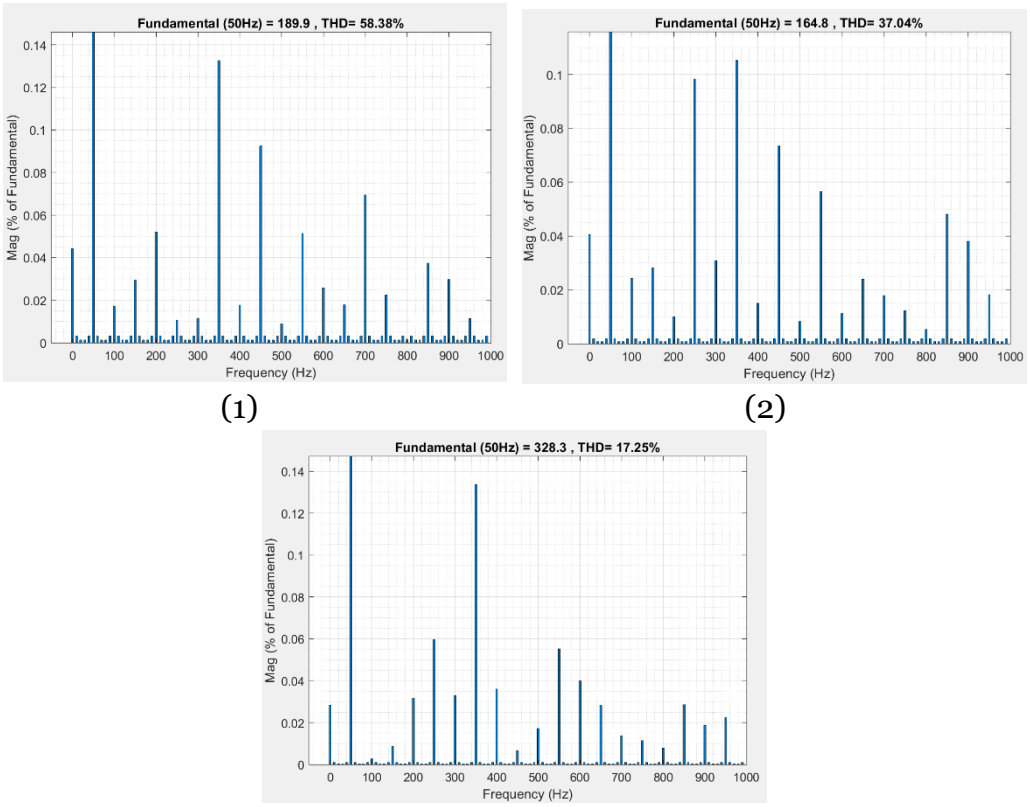


(1) (2)

Fig. 15. Line voltage of neutral point clamped three-phase (1) three-level (2) five-level

As the number of phases and levels increases, the total harmonic distortion decreases, as illustrated in Figures 16.

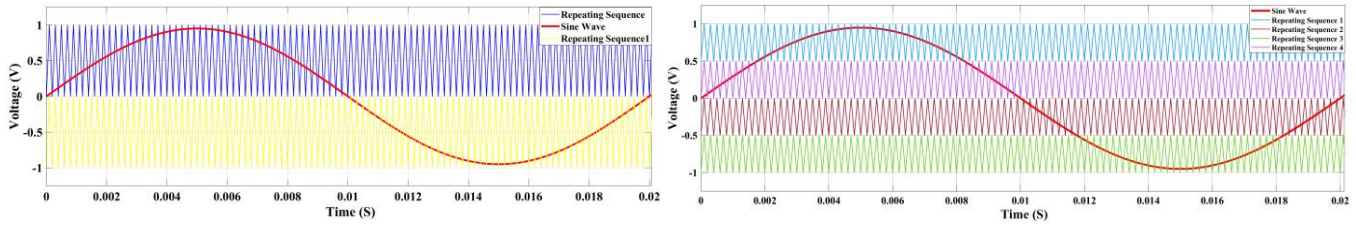


(1) (2)

(3)

Fig. 16. Total harmonic distortion of neutral point clamped inverter (1) three-level single phase (2) three-level three-phase (3) five-level three-phase

Figures 17 show the SPWM for the FC three-level and five-level configurations.



(1) (2)

Fig. 17. SPWM of the flying capacitor topology (1) three-level (2) five-level topology

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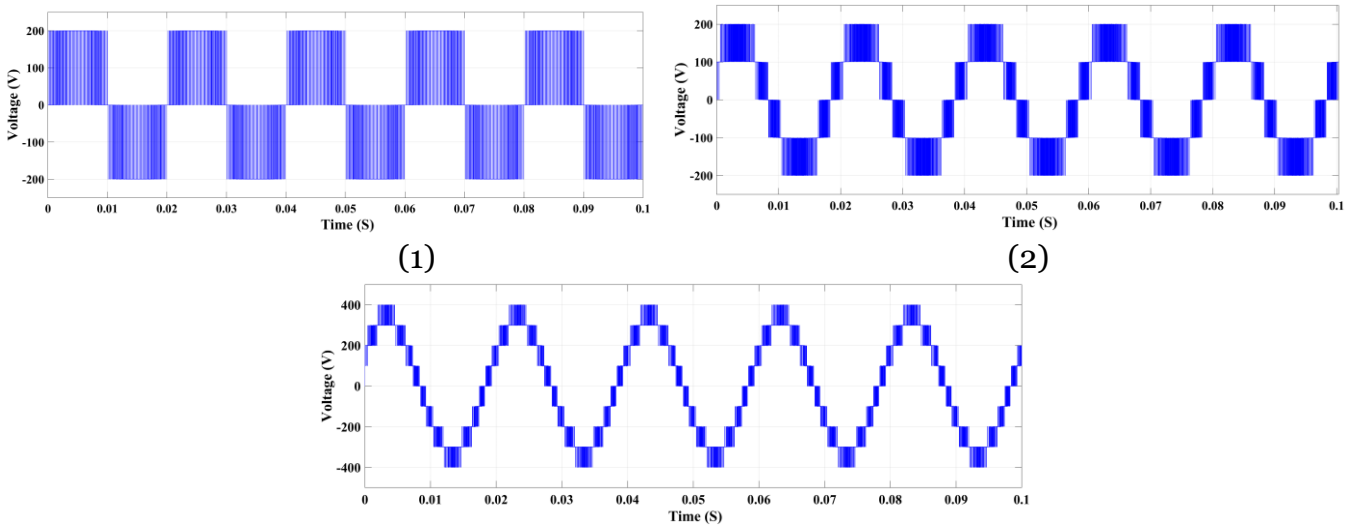
Figure 18 shows the output voltage generated by the flying capacitor inverter.

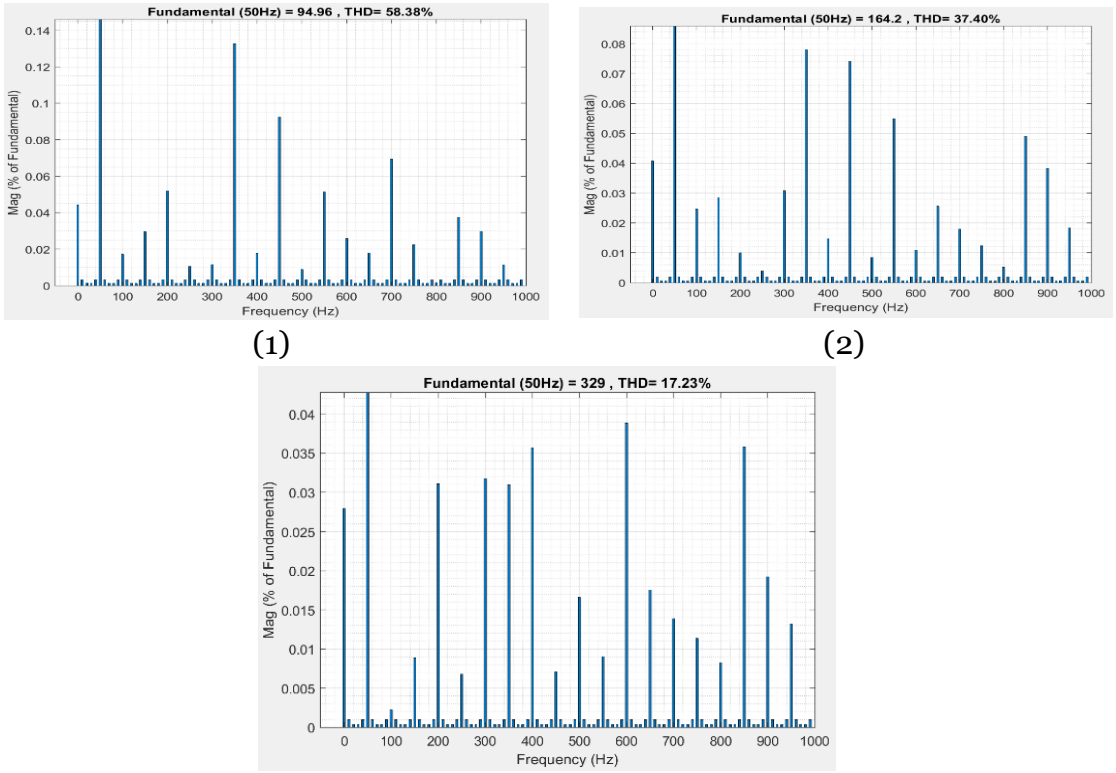


(1) (2)

(3)

Fig. 18. Output voltage of flying capacitor inverter (1) three-level single phase (2) three-level three-phase (3) five level three phase

Figures 19 illustrate that Total Harmonic Distortion (THD) reduces with increased levels and phases.



(1) (2)

(3)

Fig. 19. Total harmonic distortion of the flying capacitor inverter (1) three-level single phase (2) three-level three-phase (3) five- level three phase

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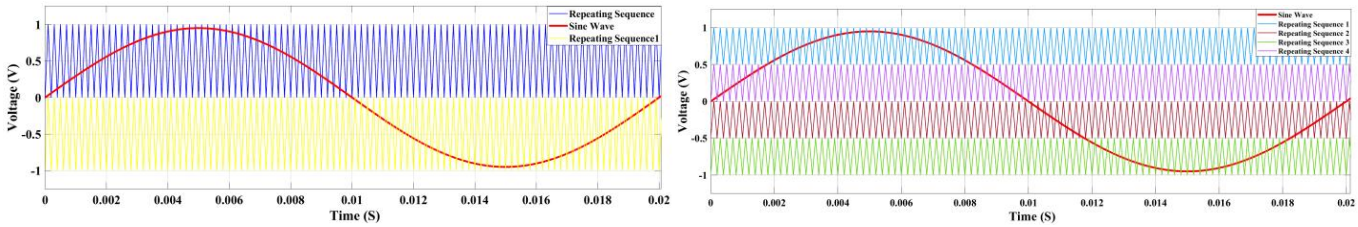
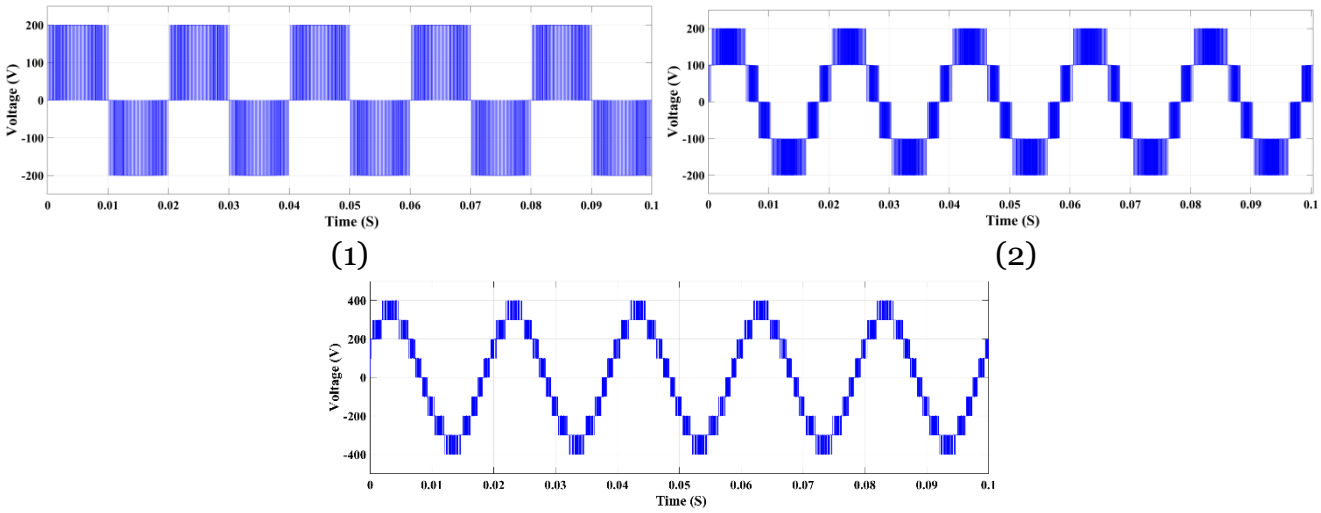
Figures 20 illustrate the SPWM of the CHB three-level and five-level configuration.



(1) (2)

Fig. 20. SPWM of the cascaded H-bridge topology (1) three-level (2) five-level

Figure 21 shows the output voltage generated by the cascaded h b bridge inverter.

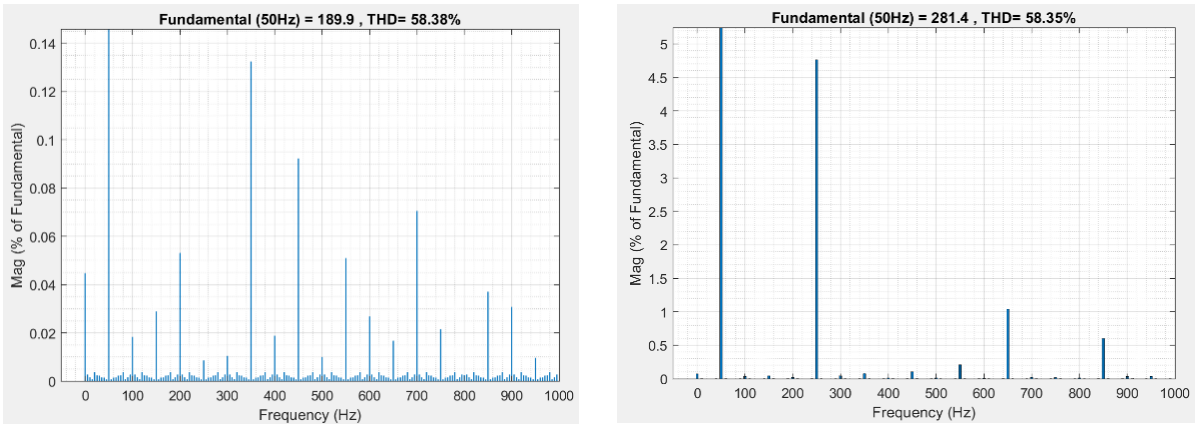


(1) (2)

(3)

Fig. 21. Output voltage of cascaded h bridge inverter (1) three-level single phase (2) three-level three-phase (3) five level three phase

The Total Harmonic Distortion (THD) decreases as the number of levels and phases increases, as illustrated in Figure 22.



(1) (2)

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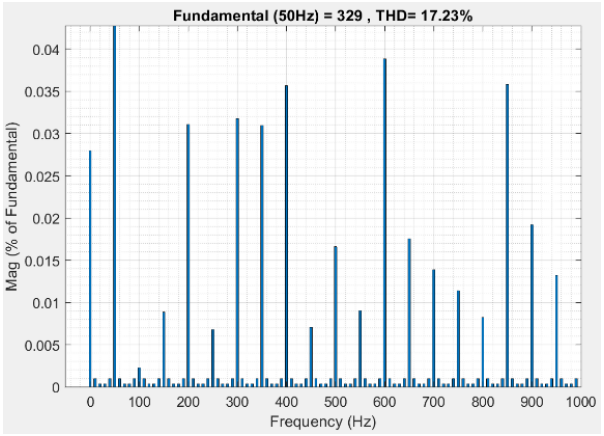

(3)

Fig. 22. Total harmonic distortion of the cascaded h bridge inverter (1) three-level single phase (2) three-level three-phase (3) five- level three phase

Figure 23 illustrates the output current and voltage of the packed U-cell 5 topology.

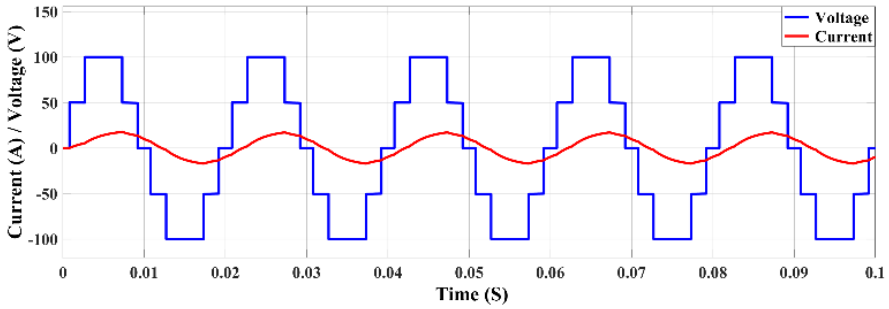

Fig. 23. Output current and voltage of the packed U cell topology

Figure 25 demonstrates a reduction in THD from 17.52, as seen in Figure 24, to 1.73 after implementing the PID

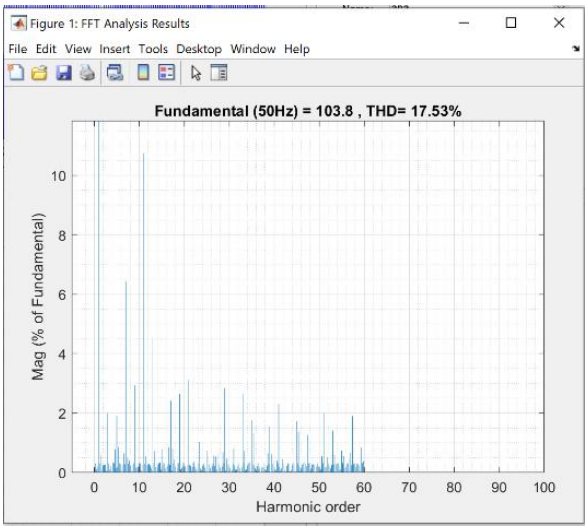

Fig. 24. FFT Analysis of the Output Voltage of the PUC5 Inverter

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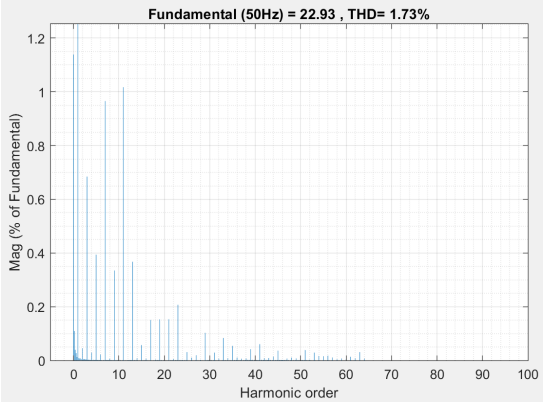

Fig. 25. FFT Analysis of the Output Voltage of the packed U cell 5 Inverter with PID Control.

Figure 26 demonstrates a reduction in THD from 17.52, as seen in Figure 24, to 1.43 after implementing the Fuzzy logic control.

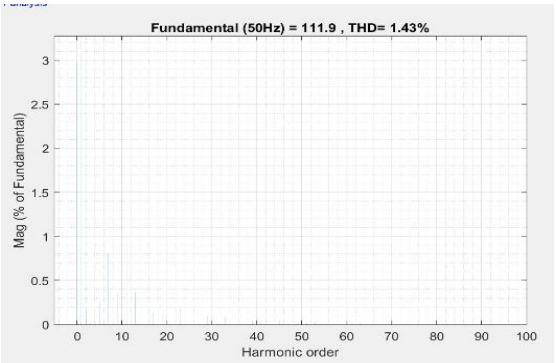

Fig. 26. FFT Analysis of the Output Voltage of the packed U cell 5 Inverter with Fuzzy logic control.

Table 9 presents the voltage's total harmonic distortion for popular inverters.

Table 9. Total harmonic distortion between inverters

Inverters	Total harmonic distortion voltage in ٪
three level single phase CHB, FC, and NPC inverters	**58,4**
three level three phase CHB, FC, and NPC inverters	**37,4**
five level three phase CHB, FC, and NPC inverters	**17,2**
Packed U-cell 5 inverter	**17,5**
Packed U-cell 5 with PID controller	**1,7**
Packed U-cell 5 with Fuzzy logic control	**1.4**

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DISCUSSION

This study provides an extensive analysis of four types of multilevel inverters: packed U-cell (PUC), flying capacitor, cascaded H-bridge, and neutral point clamped inverters, focusing on their performance in terms of total harmonic distortion (THD) and system complexity. The research began with a comparative analysis of different inverter configurations, including three-level single-phase, three-level three-phase, and five-level three-phase inverters, which significantly reduced THD for FC, CHB, and NPC converters. However, these systems required additional components, such as diodes and capacitors, which increased complexity and decreased efficiency. To address these challenges, the study introduced the packed u-cell five inverter (puc5), which maintained similar low THD levels but required fewer components, leading to greater efficiency and more straightforward implementation. The use of PID control reduced the THD to 1.7%, while fuzzy logic control further lowered it to 1.43%, demonstrating the inverter's efficiency even under high-power conditions. The findings highlight the PUC5 inverter as a superior alternative to traditional multilevel inverters, offering a promising solution for future power electronics developments. The study emphasizes the importance of balancing performance, low harmonic distortion, and reduced component count, with future research focusing on optimizing control strategies and implementing the PUC5 inverter in various applications.

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