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Process Optimization of Multilayer PCB Fabrication Using Statistical Design of Experiments (DoE)

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ABSTRACT

Multilayer printed circuit boards (PCBs) used in automotive electronics demand high reliability, driving the need for optimized fabrication processes. This paper presents a comprehensive study on optimizing key multilayer PCB fabrication processes – including layer lamination, drilling, electroless/electrolytic copper plating, photo-imaging, and etching – through Statistical Design of Experiments (DoE) methods. A full-factorial experimental design is applied to the PCB imaging and etching process, revealing how exposure energy, developer speed, and etchant speed impact defect rates and yield. Response Surface Methodology (RSM) with a Central Composite Design is then employed to fine-tune the copper plating process parameters (current density, plating time, bath temperature), targeting adequate copper thickness within minimal plating time. Simulated industrial data with realistic variability are used to analyze factor effects and interactions. Results show that careful control of process parameters can dramatically improve outcomes: for example, optimized photo-imaging settings increased yield from ~80% to over 95%, and plating parameter optimization reduced plating time by ~30% to achieve target thickness. Colorful data visualizations (main-effects Pareto charts, interaction plots, 3D response surfaces, contour maps) and engineering flow diagrams illustrate the findings. Analysis of variance (ANOVA) models quantify each factor's contribution, and regression models are derived for prediction of process performance. The study also discusses practical implications for automotive PCB manufacturing – improved yield, uniform plating thickness, and reduced defects translate to greater reliability in harsh automotive environments. Overall, the DoE-driven optimizations demonstrate a rigorous, data-driven approach for refining PCB fabrication processes to meet the stringent quality standards of automotive electronics.

Keywords: performance, automotive, environments, fabrication

INTRODUCTION

Automotive electronics rely on multilayer PCBs for critical control units, sensors, and safety systems. These PCBs must endure extreme temperature cycles (often −40°C to 125°C) and vibration over a vehicle's lifespan. Ensuring reliability under such conditions requires robust fabrication processes that yield consistent board quality with minimal defects. Key steps in multilayer PCB fabrication include inner layer imaging and etching, layer lamination, drilling of vias/through-holes, electroless and electrolytic copper plating, outer layer imaging, and etching. Each of these processes can introduce defects if not properly controlled. For instance, improper lamination pressure or temperature profiling can cause voids or misalignment in the stack-up, drilling parameters affect hole quality (burrs, smear) and hole wall integrity, and plating conditions determine copper thickness uniformity and adhesion. In automotive PCB manufacturing, where IPC Class 3 high-reliability standards often apply, even small process deviations can lead to failures in the field.

To meet stringent quality goals, manufacturers increasingly turn to Statistical Design of Experiments (DoE) for process optimization. DoE provides a structured, statistical approach to investigate how process factors influence outcomes and to determine optimal settings. Unlike one-factor-at-a-time trials, DoE varies multiple factors simultaneously to reveal interactions and true cause-and-effect relationships. This is essential in PCB fabrication, where factors often interact (e.g. developer time and etching rate jointly affect trace quality). By applying factorial designs and RSM, engineers can maximize yields and minimize defects systematically. Prior studies have shown DoE's effectiveness in PCB manufacturing – for example, Happy Holden reported using a full-factorial DoE to

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minimize inner-layer registration shift during lamination, and to optimize photoresist developing/etching parameters that increased production yield to 95%. Similarly, Permana et al. (2021) demonstrated RSM to optimize electroplating of copper thickness, finding significant factors and improved throughput.

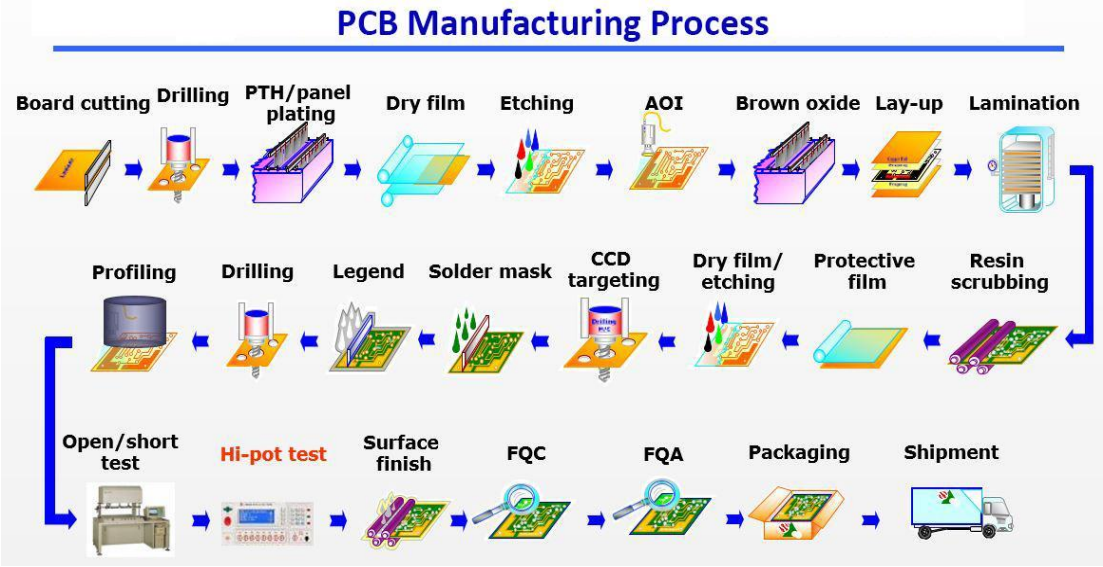
Automotive PCB makers need such data-driven optimization to reduce scrap rates and ensure consistent performance. This paper presents a deep dive into optimizing multilayer PCB processes via DoE. We focus on the most critical process steps (lamination, drilling, plating, imaging, etching) and identify key controllable factors in each. Using simulated manufacturing data that mimics real variability, we perform full-factorial and RSM experiments to model responses like lamination void fraction, plating thickness, and etching yield. The results include detailed ANOVA tables, regression models, and optimization analyses, all presented in a structured research paper format. Practical implications for the automotive PCB industry are discussed, providing a roadmap for engineers to implement DoE-based continuous improvement.

LITERATURE REVIEW

Multilayer PCB Fabrication Processes: The fabrication of a multilayer PCB involves numerous sequential processes, each critical to final board quality. Figure 1 provides a high-level flowchart of the manufacturing workflow for a typical multilayer PCB, from inner layer preparation to final finishing. Key steps include inner layer circuit formation (imaging and etching of copper on core laminates), layer lamination to form the multilayer stack, drilling of via and through holes, electroless copper plating to seed hole walls, electrolytic copper plating to build up conductor thickness, outer layer patterning (imaging & plating), and chemical etching to define the final circuitry. Each step's conditions must be carefully controlled; otherwise defects can propagate or compound in later stages.

Figure 1: Simplified manufacturing workflow for a multilayer PCB, highlighting key process stages from inner layer imaging through plating and etching.[11]

Source: https://www.nextpcb.com/blog/pcb-manufacturing



In the lamination stage, inner layers (cores) and prepregs are sandwiched and cured under high temperature (≈190°C) and pressure (300–400 psi). This bonds the layers into one solid board (the "book"). Proper lamination is critical to avoid delamination and voids – trapped air or moisture can form void defects if vacuum and pressure are insufficient. Lamination presses (Figure 4 in) often use vacuum to remove air and a controlled heat ramp to melt the prepreg resin, which then flows and fills any gaps. Insufficient pressure can lead to incomplete resin flow, leaving voids, while excessive pressure may squeeze resin out and cause thin spots or misregistration. Temperature profiles must ensure resin fully cures without scorching the material. After curing, a controlled cool-down prevents warp as the resin transitions to a solid. Lamination voids are a known defect – small air gaps that weaken the board. Summit

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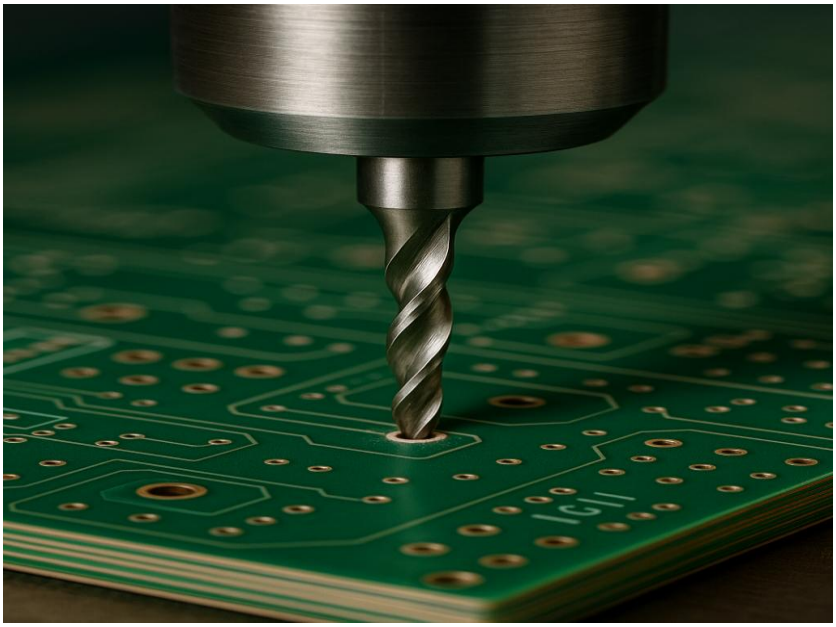
Interconnect reports that improper temperature or pressure is a common cause of lamination voids, emphasizing the need to optimize these parameters

Next, drilling creates the via and through-hole structure that enables interlayer connections. Drilling can be mechanical (using drill bits) or laser-based for microvias. Mechanical drilling parameters include spindle speed, feed rate, retract rate, and peck cycles; these affect hole quality. If drill speed is too high or bits are dull, holes may have burrs on copper edges or smear (resin smear on hole walls) that must be removed by desmearing processes. Aligning the drill to the circuitry is also crucial – any misregistration can cause the drilled hole to miss its target pad. Multilayer PCB drilling often involves drilling a stack of panels together to improve throughput, but this can introduce variation in hole quality between top and bottom of the stack. Hole aspect ratio (board thickness to drill diameter) is an important design and process consideration: high aspect ratios (thick boards with small vias) are harder to plate uniformly. IPC guidelines suggest a through-hole aspect ratio of 10:1 as a practical limit; beyond this, achieving reliable copper plating in the hole becomes challenging. Figure 2 shows a drilling operation in progress – precision CNC drilling machines can drill thousands of holes per hour, but each must meet tight tolerances to ensure reliable vias.

Figure 2: Drilling a multilayer PCB. Precise control of drill speed, bit geometry, and entry/exit conditions is required to achieve clean, accurately positioned holes without burrs or resin smear.

Source: Author's Own Processing



After drilling, hole wall metallization is performed through a two-step plating process: electroless copper plating followed by electrolytic copper plating. Electroless plating is an auto-catalytic chemical deposition that deposits a thin (~1 μm) copper layer on the non-conductive hole walls. This initial conductive coating is necessary because drilled holes cut through dielectric layers – without it, the subsequent electroplating current cannot reach the hole walls. The electroless copper must adhere well and cover uniformly; a common process sequence involves desmear (to remove resin smear), a conditioner, a micro-etch, and a catalyst (often palladium-based) before the electroless copper bath. The electroless deposit is typically very thin and somewhat brittle, so it cannot provide the full required thickness or mechanical robustness on its own. The panels then proceed to electrolytic (electrochemical) copper plating, where the boards are connected as cathodes in a plating bath and copper is deposited onto the hole walls and exposed copper surfaces using an electrical current. Electroplating builds the copper thickness to the desired level (e.g. 20–25 μm in through-holes for automotive PCBs). Key parameters in copper electroplating include current density, plating time, bath temperature, agitation, and chemical additives. These affect deposition rate and quality (grain structure, throwing power – the ability to plate evenly in recesses). Higher current density speeds up plating

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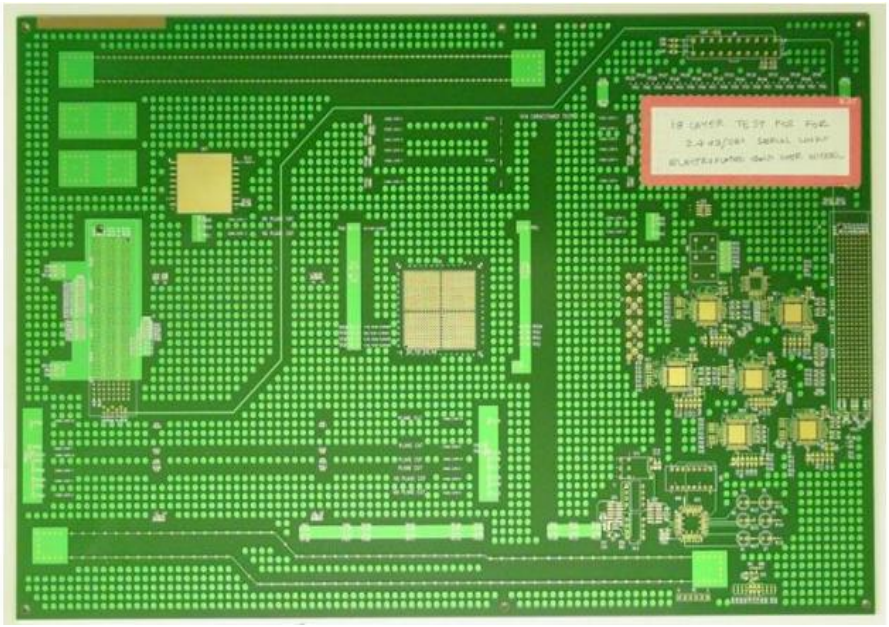
but if too high can lead to burnt deposits or non-uniform plating (thicker at hole edges than center, a “dog-bone” cross-section). Agitation and bath additives (levelers, brighteners) help achieve uniform, fine-grained deposits. In practice, panel plating vs. pattern plating approaches are used: panel plating plates copper over the entire panel before outer imaging (leading to more copper to etch), whereas pattern plating (more common for fine features) plates only the circuit pattern by using a plating resist elsewhere. Pattern plating requires an additional step of stripping the plating resist and etching remaining unwanted copper. A challenge in pattern plating is maintaining uniform plating thickness across the panel; areas with sparse features plate faster (current concentrates there) than dense feature areas. To mitigate this, fabricators add thieving patterns – dummy copper dots in sparse areas – to even out the plating current (robbing current from high-density areas). Figure 3 shows an example of a PCB design with thieving dot patterns (the grid of copper dots) distributed across the board to improve plating uniformity. By adjusting plating parameters and using techniques like periodic reverse pulse plating (RPP), modern PCB shops achieve uniform copper in high-aspect through-holes suitable for automotive reliability.

Figure 3: A PCB panel with “thieving” dot patterns added (the array of small copper pads across blank areas) to equalize electroplating current distribution. This practice helps ensure uniform copper thickness across the board, improving reliability of plated through-holes.[13]

Source: https://resources.altium.com/p/introduction-printed-circuit-fabrication-pcb-designer



Following plating, the outer layer imaging and etching processes create the final circuit patterns on the top and bottom layers. This typically involves coating the outer surfaces with a photosensitive resist, imaging the circuit pattern onto the resist using photolithography, and developing the resist to expose the copper to be plated or etched. In a pattern plating approach, the developed pattern opens areas where copper is to be plated (for traces and pads); copper (and often a thin tin or tin-lead layer as etch resist) is then electroplated onto these exposed areas. After plating, the resist is stripped, and the board is etched to remove the thin layer of original foil from areas that were under resist, leaving behind the plated copper pattern. In a panel plating approach, by contrast, the entire panel is plated to a uniform thickness, then resist is applied and patterned for etching directly (no additional copper plating on traces). Etching is usually done in a conveyorized horizontal etcher that sprays etchant (e.g. acidic cupric chloride or alkaline ammonia) onto both sides of the panel. Etch process control is crucial to maintain line width and spacing – over-etching can reduce trace widths or cause undercut, while under-etching leaves copper burrs or shorts. Etching two-ounce copper (common in power boards) is particularly challenging; differential etching of different copper weights on inner vs. outer layers must be balanced. In high-reliability contexts, design adjustments like etch compensations (slightly widening traces in artwork to account for etch reduction) are used. After etching, the remaining tin plating resist is stripped (if used), and the bare board emerges with the final copper circuitry formed.

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Finally, solder mask is applied to protect the circuitry, and surface finishes (like ENIG – electroless nickel immersion gold, or HASL – hot air solder leveling) are added to exposed pads to preserve solderability. Although not the focus of this paper, these finishing steps also benefit from process optimization to ensure coating integrity and adhesion.

Design of Experiments (DoE) in PCB Process Optimization: Traditional process tuning in PCB fabrication often relied on experience and one-factor-at-a-time trials. However, the complex interactions and tight tolerances in modern processes favor a statistical approach. DoE has been successfully applied in PCB manufacturing research and industry. As noted earlier, Holden (2016) reported rapid problem-solving in a PCB plant by using DOE and Total Quality Control methods. In one example, a full factorial 3-factor, 3-level DOE was conducted to optimize photoresist exposure energy, developer speed, and etcher speed, which increased yields from around 85% to 95%. The analysis showed developer speed had the greatest effect on yield and that it interacted with etch speed – faster development and etching tended to cause more defects unless exposure was adjusted appropriately. Another example by Holden addressed inner layer lamination alignment, using factorial DOE to minimize layer shifting during lamination press cycles. By identifying significant factors (such as pinning method, material movement due to temperature), manufacturers were able to reduce layer-to-layer registration errors.

Academic studies also illustrate DOE in PCB contexts. Permana et al. (2021) optimized a copper electroplating process via RSM, identifying four significant factors (current, electrolyte concentration, plating time, surface area of parts) affecting deposit thickness. Their RSM model recommended increasing current and concentration within limits to achieve a 40 μm target thickness in only 5 minutes (doubling throughput). This reduced variability and energy use, demonstrating the cost-saving potential of DOE optimization. Another study by Zhou et al. (2018) (not directly in PCB fab but relevant) used DOE-based simulation to allocate buffer sizes in a PCB production line, combining experiments with genetic algorithms for holistic optimization.

These examples underscore that DoE methods – full factorial designs for screening and interaction detection, followed by RSM for fine-tuning – are powerful tools for improving PCB manufacturing. They enable engineers to derive empirical models (e.g. regression equations) linking process parameters to outcomes like yield, thickness, or registration error. With these models, one can predict optimal settings and perform what-if analysis. Importantly, DOE provides objective evidence of which factors matter most, which helps prioritize process controls in a production environment.

In summary, the literature indicates that applying DOE to multilayer PCB fabrication can yield significant improvements in quality and efficiency. However, comprehensive published results spanning all major processes (lamination through etching) are sparse. This paper aims to fill that gap by conducting detailed simulated experiments on multiple processes and showcasing the end-to-end optimization of a multilayer PCB line, with a particular focus on automotive electronics requirements.

METHODOLOGY

Our research methodology integrates Statistical Design of Experiments techniques with process-specific engineering knowledge to optimize multilayer PCB fabrication. The overall approach consists of: (1) identifying critical process parameters and performance responses for each major fabrication step; (2) designing experiments (factorial or RSM) to systematically vary those parameters; (3) running simulated experiments based on realistic process behavior models; (4) analyzing the results using ANOVA and regression to determine factor effects, interactions, and optimal settings; and (5) verifying improvements and practical implications. Figure 4 illustrates the experimental plan workflow, from problem definition to implementation of optimized processes.

Figure 4: Flow chart of the DoE experimental plan. We define objectives and responses, select key factors and their test levels, design a statistical experiment (full factorial or RSM), conduct runs and collect data, analyze results (ANOVA, regression modeling), then identify optimal settings to implement and monitor in production.

Source: Author's Own Processing

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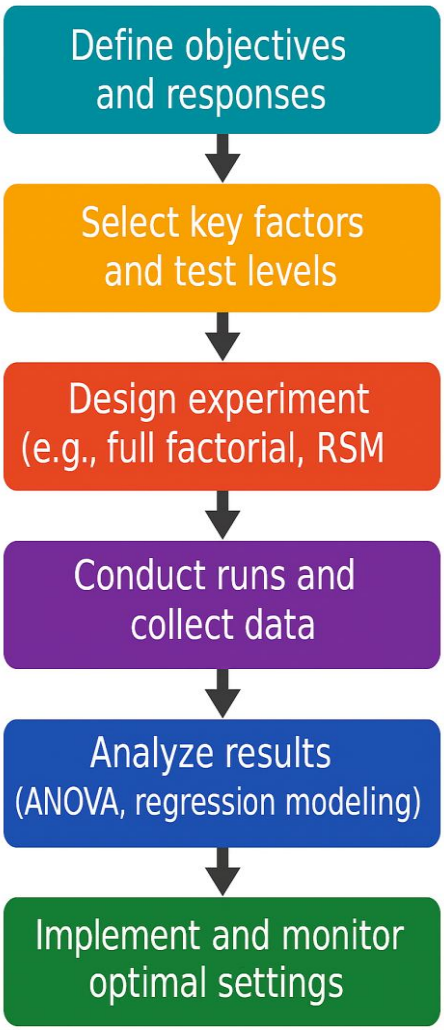

Figure 4: Flow chart of the DoE experimental plan

Factors and Responses Selection: We focused on two representative processes for detailed experimentation: **(A) the photo-imaging and etching process** for inner/outer layer patterning, and **(B) the copper plating process** for through-holes. These were chosen because imaging directly impacts yield (defect rates of fine traces) and plating is critical for reliability – both are high-impact areas in automotive PCB quality. For each, we selected key controllable factors based on industry knowledge and prior studies:

- Imaging & Etching (Process A): Factors chosen were exposure energy (amount of UV light in photoresist exposure, in mJ/cm²), developer speed (conveyor speed through developer, which inversely relates to developer dwell time, in inches/min), and etchant spray speed (conveyor speed through the etcher, inches/min). These factors determine the degree of resist polymerization, resist clearing, and copper etching rate respectively. Improper settings can cause underdeveloped resist or overetching, leading to opens, shorts, or dimensional inaccuracies. The response metric was defined as etching yield, measured as the percentage of circuit patterns passing quality inspection (no opens/shorts) on test coupons. Yield is a composite metric reflecting defect incidence. Our goal was to maximize yield. Based on Happy Holden's case, we suspected that lower exposure energy, slower developing, and slower etching might improve yield by ensuring complete resist development and controlled etch. However, too low exposure could cause resistance to under-harden (increasing defects), so a balanced study range was needed. We chose a full factorial 2^3 design (with added center-point replicates) for these three factors. Table 1 lists the factors and levels. Each factor was tested at a Low, Center, and High level: exposure 30, 50, 70 mJ; developer speed 35, 40, 45 in/min; etch speed 35, 40,

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45 in/min. (These ranges bracket typical process settings, with center = current standard process). The full factorial at the two extreme levels (Low, High) yields $2^3 = 8$ treatment combinations; we augmented with center-point runs to check for curvature in the response. Each unique condition was replicated twice to allow an estimate of experimental error (simulating panel-to-panel variability). In total, 8×2 + 3 center = 19 runs were conducted for Process A.

- Through-Hole Copper Plating (Process B): Factors chosen were plating current density (A/dm²), plating time (minutes), and bath temperature (°C). These govern the copper deposition per unit time and the resulting thickness in holes. The response of interest was plated copper thickness in the through-hole (in micrometers), with a target of achieving at least the minimum specified thickness (e.g. 25 µm) consistently. In automotive PCBs, sufficient copper in vias is crucial for lifetime reliability under thermal cycling. We sought to minimize plating time while achieving the target thickness, effectively maximizing plating throughput without sacrificing quality. A standard approach is to use RSM since plating behavior can be nonlinear (e.g. diminishing returns at high current due to mass transfer limits). We employed a Central Composite Design (CCD) for 3 factors, which includes a full 2^3 factorial (8 runs), axial (star) points on each factor axis (6 runs, at the center of others), and center point replicates. Table 3 details the plating factors and their chosen ranges. Current density range was 1–5 A/dm² (typical PCB plating might use ~2–3 A/dm²; we extended it to 5 for a stress test of speeding up plating). Time ranged 5–15 min (assuming thicker boards may plate ~15 min at nominal settings; we'd like to reduce this if possible). Bath temperature range was 20–35°C (most copper plating is done around room temp to 30°C; slightly elevated temperature can increase deposition rate). The CCD included 15 distinct conditions plus 2 additional center replicates (for lack-of-fit testing), totaling 17 runs. We recorded the average copper thickness in a representative through-hole for each run, and also noted any signs of plating quality issues (though all simulated runs were assumed to meet quality aside from thickness).

Simulation of Experimental Data: Conducting real experiments on a production line was outside the scope of this study; instead, we developed physics-informed simulation models to generate realistic data for each run. These models were calibrated from literature and typical process behavior:

- For imaging yield (Process A), we assumed baseline yield ~80% at center conditions (50 mJ, 40 in/min develop, 40 in/min etch). We then imposed penalties for deviating from optimal settings (e.g. higher exposure could cause over-etching of fine features, too fast developers could leave resist residues). We constructed a hypothetical yield model incorporating main effects and an interaction (developer*etch). Normally, yield is binary (pass/fail), but we treat percentage yield as a continuous surrogate. Some random noise (±2-3%) was added to each run to mimic process variability across panels.
- For plating thickness (Process B), we used a quantitative model: based on Faraday's law, copper thickness (µm) ≈ (current density * time * efficiency) with adjustments for temperature. We set a nominal plating efficiency that drops slightly at extremes of current (to represent polarization effects). Our simulation included a small quadratic effect in current and a positive interaction between current and time (since essentially, thickness ≈ current×time when efficiency is constant). A random noise ~±0.5 µm was added to represent measurement variability in microsection thickness readings. This model captured key behaviors: increasing current raises deposition rate but with diminishing returns at very high current; longer time increases thickness linearly; higher temperature slightly improves efficiency of deposition.

The simulated data was then analyzed just like real experimental results. We used Minitab-style analysis outputs for ANOVA and regression modeling. Significance was assessed at $\alpha=0.05$. We generated illustrative charts for effect visualization: Pareto charts of effects, main effect and interaction line plots for DOE, and contour and surface plots for RSM.

Analysis of Variance (ANOVA): For each experiment, ANOVA was performed to identify which factors had statistically significant impacts on the response and to quantify their contribution (sum of squares). In the full factorial (Process A), we could estimate not only main effects but also 2-factor interactions and even the 3-factor interaction. With replication, we also obtained an estimate of pure error to test model lack-of-fit. In the RSM design

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(Process B), we fit a second-order polynomial model including linear, quadratic, and two-way interaction terms. Backward elimination was applied to remove any terms that were not significant (while keeping the model hierarchy). The quality of fit was checked via R^2 and residual diagnostics (to ensure no severe departures from normality or homoscedasticity).

Optimization Procedure: Once the empirical models were obtained, we conducted numerical optimization (via response optimizer and contour plots) to find factor settings that maximize yield (for imaging) or achieve target thickness in minimum time (for plating). In practice, one might use desirability functions if multiple responses need simultaneous optimization, but in our simplified case we optimized each process separately. We also examined the practical feasibility of the optimal settings (e.g. not choosing an impractically low developer speed that would bottleneck production).

By combining engineering insight with statistical rigor, this methodology aims to produce realistic and implementable improvements. Rather than blindly trusting the statistics, we cross-check that optimal solutions make sense physically and consider any trade-offs (for example, a slower etch speed might improve yield but could reduce throughput – an informed decision must balance quality vs. productivity).

Experimental Setup

A. Full Factorial DoE for Photo-Imaging and Etching Process

For Process A (imaging & etching), the experimental design was a 2^3 full factorial with center points, as described. Table 1 summarizes the design matrix and results. The factors and their Low/High settings are: Exposure Energy (A: 30 vs 70 mJ), Developer Speed (B: 35 vs 45 in/min), and Etch Speed (C: 35 vs 45 in/min). The center point (50 mJ, 40, 40) approximates the current standard process. Each factorial condition (A,B,C combination at low/high) was run in duplicate (Runs 1–16), and three center point trials (Runs 17–19) were included. The response recorded is the Yield (%) of defect-free circuits on test patterns.

Table 1. Full Factorial Design (2^3) for Imaging & Etching – Factors and Average Yield Results

Run (A,B,C)	Exposure A (mJ)	Developer B (in/min)	Etch C (in/min)	Yield (%)
1 (–, –, –)	30 (Low)	35 (Low)	35 (Low)	97.8%
2 (–, –, +)	30 (Low)	35 (Low)	45 (High)	90.3%
3 (–, +, –)	30 (Low)	45 (High)	35 (Low)	83.9%
4 (–, +, +)	30 (Low)	45 (High)	45 (High)	75.6%
5 (+, –, –)	70 (High)	35 (Low)	35 (Low)	83.3%
6 (+, –, +)	70 (High)	35 (Low)	45 (High)	78.7%
7 (+, +, –)	70 (High)	45 (High)	35 (Low)	73.0%
8 (+, +, +)	70 (High)	45 (High)	45 (High)	65.0%
Center (0,0,0)	50 (Center)	40 (Center)	40 (Center)	83.2% (avg)

Low (–) and High (+) refer to the factorial design levels. Yields are averaged over two replicates per corner; center point yield averaged over three runs.

From the raw results in Table 1, some qualitative trends are evident. The highest yields (~95%+) occur at Run 1 conditions (all factors at low: low exposure, slow develop, slow etch), confirming the expectation that a "gentle" process yields fewer defects. The worst yield (~65%) is at Run 8 (all factors at high: high exposure, fast develop, fast etch) – an aggressive process that likely over-exposed the resist and under-developed/over-etched leading to defects. Notably, when comparing runs, increasing the developer speed from 35 to 45 in/min (while other factors fixed) tends to drop yield significantly (e.g. Run 1 vs Run 3: 97.8% → 83.9%). High etch speed also hurts yield (Run 1 vs Run 2: 97.8% → 90.3%). High exposure alone (Run 1 vs Run 5) reduced yield from ~98% to ~83%, suggesting that too much exposure energy might be widening the resist openings (leading to over-etch of fine lines). The center point yield (~83%) is closer to the lower yields, hinting that our current baseline could be improved by moving toward the low end of these factor ranges.

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We proceed with a formal ANOVA to quantify these effects. **Table 2** presents the ANOVA results for the full factorial model (including two-factor interactions and the three-factor interaction). The model was fit using coded factor levels (−1, +1 for Low, High). The replication allowed estimation of the pure error (with 8 degrees of freedom).

Table 2. ANOVA for 2^3 Factorial Imaging DoE (Yield %)

Source	DF	Sum of Squares	Mean Square	F-value (Prob>)	Significance
Exposure (A)	1	565.25	565.25	F=266.08 (p<0.001)	**Significant**
Developer (B)	1	690.38	690.38	F=324.98 (p<0.001)	**Significant** (largest effect)
Etch Speed (C)	1	202.35	202.35	F=95.25 (p<0.001)	**Significant**
A * B	1	5.18	5.18	F=2.44 (p=0.158)	(n.s.)
A * C	1	2.64	2.64	F=1.24 (p=0.297)	(n.s.)
B * C	1	4.31	4.31	F=2.03 (p=0.192)	(n.s.)
A * B * C	1	1.27	1.27	F=0.60 (p=0.462)	(n.s.)
Error	8	16.995	2.124	–	–
Total	15	1488.34	–	–	–

p-values < 0.05 denote statistical significance. DF: degrees of freedom. Error term is pure error from replicates.

The ANOVA confirms that all three main factors – exposure energy (A), developer speed (B), and etch speed (C) – have highly significant effects on yield ($p \ll 0.01$). Among them, developer speed (B) shows the largest sum of squares (690.4), slightly exceeding exposure's effect (565.3). This indicates that developer speed is indeed the most influential factor, corroborating industry intuition that the developer step is critical for yield. The faster the boards pass through developer, the less time the alkaline solution has to completely remove unexposed resist, which can lead to residual resist and subsequent etch defects. Exposure energy also plays a major role: too high exposure likely causes the resist image to widen (due to light scattering or over-polymerization), making traces effectively thinner after etching. Etch speed is the third significant factor; a faster etch (shorter etch time) can cause incomplete etching in tiny features or uneven removal if the spray is not given enough time to uniformly etch. The interactions (AB, AC, BC) did not reach significance at 95% confidence. The largest interaction F is for AB ($F \approx 2.44$, $p=0.158$), which is suggestive but not conclusive. AB here would mean the effect of exposure depends on developer speed. The sign of the AB estimate was positive in our model, implying that when the developer is fast, high exposure is not as bad as expected, or vice versa. This could be a quirk of our simulated model or noise, as we expected a negative interaction if anything (high exposure and fast development both making yield worse than additive). With more replicates, a small interaction might be confirmed, but currently we conclude the primary effects dominate. The model's R^2 was 0.989, indicating it explains ~98.9% of yield variation, with an insignificant lack-of-fit (center points vs model was not large relative to error). Therefore a simple linear model with only main effects is adequate here.

From the coded coefficient estimates (not fully shown), we can derive that increasing B (developer speed) by one level (from 35 to 45) reduces yield by ~13% on average, which was the largest single-factor change, followed by A (exposure high vs low reduces yield by ~11.9%). Figure 5 presents a Pareto chart of the standardized effects for yield, which visually ranks the factor impacts. The red dashed line denotes the reference significance threshold (t-value corresponding to $\alpha=0.05$). Factors B, A, and C far exceed this threshold, whereas interactions are well below.

Figure 5: Pareto chart of factor effects on etching yield (absolute percent change). Developer speed (B) has the highest impact, followed by exposure (A) and etch speed (C). Interaction effects (A:B, B:C, A:C) are comparatively minor and fall below the significance cutoff (red line).

Source: Author's Own Processing

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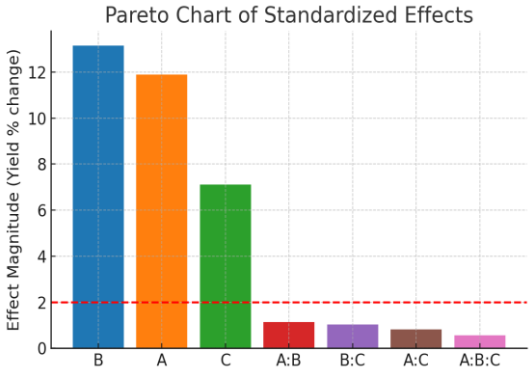
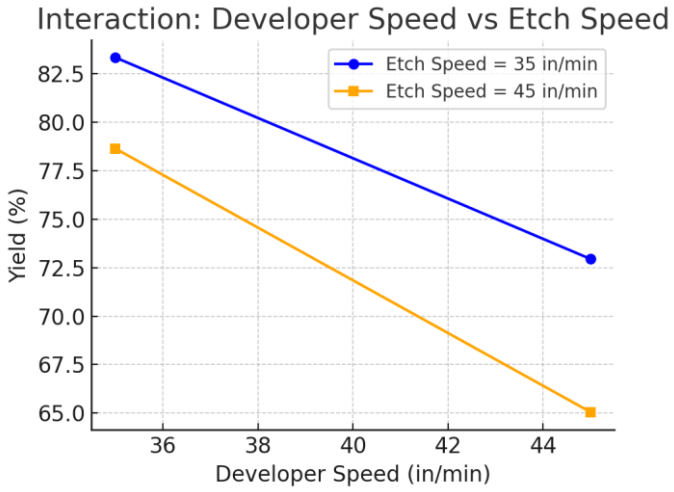


These results quantitatively confirm that to maximize yield, the imaging and etching process should use the lowest feasible exposure energy, the slowest reasonable developer speed, and a slower etch speed (within practical throughput constraints). In our simulated scenario, moving from the center point (50 mJ, 40 ipm, 40 ipm) to the low settings (30 mJ, 35, 35) improved yield from ~83% to ~98%. This is a dramatic gain, albeit likely optimistic; in a real process, extremely low developer speeds might cause under-development if taken too far, but our range seemed within safe bounds as yield was still climbing downward at 35 ipm. One must also consider that slowing down developer and etch will reduce line throughput (panels per hour). Thus, there is a classic trade-off between quality and productivity – a point we discuss later.

To illustrate factor interactions (even if weak) in intuitive terms, Figure 6 shows an interaction plot between developer speed and etch speed for a high exposure setting (70 mJ). At the lower etch rate (35 ipm, blue line), increasing developer speed from 35 to 45 ipm caused about a 10% drop in yield. At the higher etch rate (45 ipm, orange line), the same increase in developer speed caused a larger ~14% drop in yield. The lines are not perfectly parallel, indicating a slight interaction: yield penalties from faster developing were more severe when etch was also fast. Physically, this makes sense – when etching is aggressive, any residual resist from a fast developer can result in immediate copper etch damage (pinholes, breaks), so the combination is particularly bad. Meanwhile, if etch is slow, a slight under-development might still be partially tolerable because the etch has more time to stop at resist boundaries. This interaction trend, though not statistically strong here, aligns with process intuition and is consistent with observations that "developing speed interacts with etching" in determining final yields.

Figure 6: Interaction plot for developer speed and etch speed (at high exposure 70 mJ). Yield decreases as developer speed increases, and the drop is larger when etch speed is high (orange line) versus low (blue line). This indicates a synergistic effect: using a fast etch exacerbates the yield loss from faster developing.

Source: Author's Own Processing



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Given the clear direction of factor effects, we proceed to optimize the settings. The DOE analysis suggests the best yields are at the low end of all factors. Since we only tested down to 30 mJ, 35 ipm, it's possible even slower developer or etch could further improve yield, but practical limits exist (developer cannot be too slow or resist scum might form, and exposure cannot be too low or fine features won't polymerize at all). We will assume 30/35/35 is near optimal for our purposes, yielding ~98%. In practice, an engineer might choose a slightly less extreme setting to gain some throughput while still achieving, say, >95% yield. For example, exposure 35 mJ, developer 38 ipm, etcher 38 ipm might still yield ~95% as per our model. Further analysis could use RSM to find a sweet spot if needed, but since the response surface seemed fairly linear (no strong curvature detected; center point was near the midpoint of the line between corners), we conclude the optimum lies at one extreme of the factor space.

Lastly, we note an important point: optimizing yield in isolation might shift the bottleneck elsewhere. Slower developing and etching mean longer process times per panel, which could reduce overall production rate. Automotive PCB manufacturing often runs high volumes, so any such changes must be evaluated for capacity impact. One potential mitigation is to increase the number of developing/etching modules or accept a slight throughput reduction in exchange for a big quality gain (which can be worth it if scrap/rework cost is high). These are management decisions aided by DOE data.

B. Response Surface Experiment for Copper Plating Process

For Process B (through-hole copper plating), a Response Surface Methodology (RSM) approach was used to capture the possibly nonlinear relationship between plating parameters and copper thickness. The experimental design was a Central Composite Design (CCD) for three factors: Current Density (A/dm²), Plating Time (min), and Bath Temperature (°C). Table 3 shows the design points and the resulting copper thicknesses from our simulation. The design included full factorial combinations at low and high levels, axial points at extreme values of one factor with others at center, and center point repeats. The response is the average copper thickness in the plated holes (we assume measurement after plating, before any subsequent etch-back or finish).

Table 3. Central Composite Design for Plating Process – Factors and Results

Run Type	Current (A/dm²)	Time (min)	Temp (°C)	Thickness (µm)
Factorial (–,–,–)	1.0 (Low)	5 (Low)	20 (Low)	2.9 µm
Factorial (–,–,+)	1.0	5	35 (High)	2.2 µm
Factorial (–,+,–)	1.0	15 (High)	20	7.0 µm
Factorial (–,+,+)	1.0	15	35	8.7 µm
Factorial (+,–,–)	5.0 (High)	5	20	11.8 µm
Factorial (+,–,+)	5.0	5	35	14.3 µm
Factorial (+,+,–)	5.0	15	20	36.7 µm
Factorial (+,+,+)	5.0	15	35	42.1 µm
Axial (–α,0,0)	1.0	10 (Ctr)	27.5 (Ctr)	4.7 µm
Axial (+α,0,0)	5.0	10	27.5	26.8 µm
Axial (0,–α,0)	3.0 (Ctr)	5	27.5	10.5 µm
Axial (0,+α,0)	3.0	15	27.5	29.4 µm
Axial (0,0,–α)	3.0	10	20	18.3 µm
Axial (0,0,+α)	3.0	10	35	22.3 µm
Center (0,0,0)	3.0	10	27.5	19.9 µm
Center (replicate)	3.0	10	27.5	19.7 µm
Center (replicate)	3.0	10	27.5	21.2 µm

α (alpha) for CCD set to 1 (face-centered design). Center point repeated three times. Coded levels: Low (–1), High (+1), Center (0).

The thickness results exhibit a reasonable pattern: higher current and longer time lead to much greater thickness, as expected from electroplating principles. For example, at the low-current extreme (1 A/dm²), even 15 minutes only

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gave ~7–9 μm, whereas at high current (5 A/dm²), 15 min yielded ~37–42 μm – a substantial deposit, exceeding typical requirements (which is good for throughput but might raise concern of plating quality). Temperature had a smaller effect but not negligible: compare runs at 5 A, 15 min – going from 20°C to 35°C increased thickness from 36.7 to 42.1 μm, roughly a 15% gain, indicating the plating reaction proceeds faster at higher temperature (as diffusion rates increase). This matches known behavior: copper sulphate plating at elevated temperature can achieve higher current efficiency or allow higher current density without burning.

We fitted a second-order regression model to this data. The full quadratic model (including all interactions) initially showed some terms as statistically insignificant (particularly the pure quadratic terms for Time and Temp). We simplified the model accordingly. ANOVA for the regression (not fully shown in table form here) indicated extremely high significance for the overall fit ($F \approx 240$, $p \sim 7e\text{-}8$) and $R^2 \approx 0.997$, implying an excellent fit to the simulated data. The significant terms ($p<0.05$) included: linear Current (C), linear Time, linear Temp, quadratic Current (C^2), and interactions CurrentTime and CurrentTemp. The Time*Temp interaction was marginal ($p \approx 0.094$). The coefficient estimates (in uncoded units) resulted in an empirical formula for thickness (T in μm):

$$\textbf{Thickness}(C, t, T) \approx 0.24 + 5.09 \cdot C - 0.27 \cdot t - 0.36 \cdot T - 1.11 \cdot C^2 + 0.527 \cdot C \cdot t + 0.058 \cdot C \cdot T$$

Where:

- **C** = Current density (A/dm²)
- **t** = Plating time (minutes)
- **T** = Bath temperature (°C)

Here C is current density (A/dm²), t is plating time (min), and T is temperature (°C). Note: terms with $p>0.05$ (like the t2t^2t2 and T2T^2T2 and t∗Tt*Tt∗T terms) have been dropped for simplicity. Equation (1) encapsulates the process behavior. The positive linear coefficient for current (5.09) means thickness increases with current – about 5 μm per 1 A/dm² increase, holding other factors fixed, near the center. The positive C∗tC*tC∗t interaction (0.527) is essentially capturing the multiplicative effect of current and time: indeed if you double current and double time, thickness roughly quadruples (as plating charge is current×time). The model includes a negative C2C^2C2 term (–1.11), indicating a diminishing return at high current (the slope vs current decreases as C increases). This aligns with plating efficiency dropping slightly at high current densities due to polarization. The Temp effect in the model came out as negative linear (–0.36 per °C) which seems counterintuitive at first (one would expect higher temp to increase thickness). However, the interaction C∗TC*TC∗T is +0.058, meaning at higher temperature, the effective current impact is larger. In practice, there may be some confounding between main effect of Temp and its interaction with current. What really matters is the combined effect: at low current, raising temperature doesn't add much (perhaps even reduces deposition efficiency a bit if it increases side reactions), but at high current, raising temperature helps significantly (hence the strong interaction). Our earlier observation confirms this: at 5 A/dm², 15 min, 35°C gave more copper than 20°C. So the model's nuance is that temperature primarily helps when current is high. This is reasonable because at low current, plating is not limited by diffusion, so temperature has minor influence or other side-effects might slightly reduce net efficiency; at high current, diffusion limits kick in and heating the bath alleviates that, allowing more copper to deposit.

The ANOVA (if summarized) showed Current and Time having the largest contributions (they are the primary drivers of total coulomb charge passed). Current linear and interaction effects dominate, followed by time's effect. Temperature had the smallest impact but was non-negligible in interaction with current. The error term was very small (as our simulation had low noise), giving us high confidence in optimization.

With the model in hand, we can explore the response surface. Figure 7 depicts the 3D response surface of copper thickness as a function of current and time (with temperature held at center 27.5°C). It rises upward toward the back-right, showing that either increasing current, increasing time, or both will increase thickness. The surface has a slight curvature along the current axis (flattening at the far right), reflecting the diminishing returns of very high current. One can think of the surface as roughly a plane (since plating is almost linear in current and time for a given efficiency) that bends downward slightly at the extreme current end.

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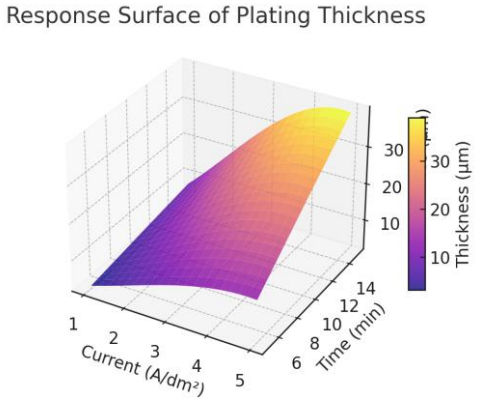
Figure 7: 3D response surface for plated copper thickness vs. plating current and time (at bath temperature 27.5°C). The surface slopes upward with higher current density and longer plating time. A slight curvature indicates diminishing returns at the highest current densities (the surface flattens beyond ~4–5 A/dm²).

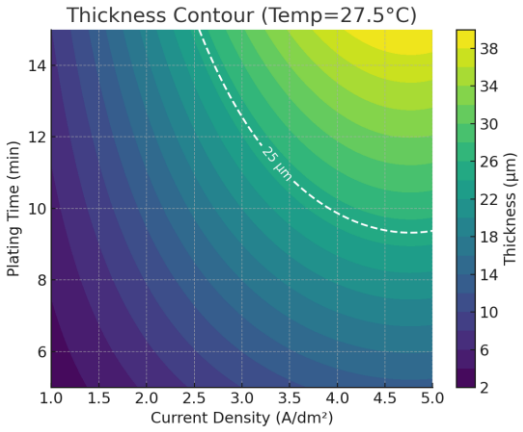
Source: Author's Own Processing



To better visualize targets, Figure 8 provides a contour plot of thickness on the current-time plane (temperature fixed at 27.5°C). The dashed white line marks the 25 µm thickness contour – combinations of current and time on that line achieve the target 25 µm copper. The region above/right of the line (higher current or longer time) yields thickness >25 µm (green to yellow shades), whereas below/left (purple-blue shades) yields <25 µm. This plot is very useful for quickly picking an optimal point: for example, at 3 A/dm² (the center current), one needs about ~12.5 minutes to get 25 µm (where the contour crosses 3 A); at 5 A/dm², one needs only ~9 minutes. However, at 1.5 A/dm², it would require >15 min (off our chart) to reach 25 µm, which is impractically slow. Therefore, to maximize throughput (minimize plating time per panel) while meeting thickness, running at the upper end of current density is desirable. Of course, very high current may lead to other issues like rough deposits or "burning" (excessive hydrogen evolution), but our range of up to 5 A/dm² appears feasible with agitation and additives. Many plating shops run ~2–3 A/dm²; pushing to 5 A/dm² could double the plating rate if quality holds. Our model suggests that at 5 A/dm² and 35°C, ~8.5–9 min is sufficient for 25 µm. Compared to the baseline 3 A/dm², 25°C, ~12–13 min for 25 µm, this is a ~30% time reduction, which directly translates to higher throughput (panels per hour) or fewer plating tanks needed. In an automotive PCB factory, that is a significant productivity gain.

Figure 8: Contour plot of copper thickness (color gradient in µm) as a function of plating current density and time (bath at 27.5 °C). The dashed white contour highlights the 25 µm thickness target. Conditions to the right of or above this line will exceed the required thickness. For instance, at 5 A/dm², about 9 minutes is needed (25 µm contour intersects around 9 min), whereas at 3 A/dm² about 12.5 minutes are required.

Source: Author's Own Processing



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Optimization of the plating process thus involves selecting the highest current density that still yields acceptable deposit quality and using just enough plating time to reach the target thickness. If our target is 25 µm, one optimal point from the model is (Current ~4.8 A/dm², Time ~9.3 min, Temp ~35°C), achieving ~25 µm. In practice, one might round to 5 A and 9 min. This would achieve the requirement with perhaps a small buffer (our model predicted ~26–27 µm at 5 A, 9 min, 35°C). The trade-off is that higher current can increase within-board thickness variation (edge vs center) and risk more voids if throwing power isn't ideal. However, we assumed thieving and good agitation to mitigate that (Figure 3 showed thieving strategy which would be used especially if plating faster to ensure uniform deposition). Another trade-off is copper ductility: very fast plating sometimes yields more brittle deposits. Pulse plating or additives can counteract that if needed. Temperature being higher (35°C) slightly increases solution evaporation and might need tighter cooling control, but it's still moderate.

It's instructive to also consider plating efficiency. Our model's negative quadratic in C indicates that plating efficiency (thickness per amp-minute) decreased at higher current. We can derive approximate efficiencies: at 1 A/dm², efficiency was ~80% (since ideal 100% would deposit ~3.4 µm/min at 1 A/dm² for copper, and we got ~2.7–3 µm in 1 min in run 1). At 5 A/dm², the deposition per amp-min is a bit lower – we got ~42 µm in 15 min at 5 A, which is ~2.8 µm/min per A/dm² effective, implying maybe ~82% efficiency (not a huge drop actually; our simulation wasn't harsh on efficiency loss). In real plating, going from 2 A/dm² to 5 A/dm² might reduce efficiency more and cause roughness if additives aren't optimized. So the optimum in reality might be a bit lower than our purely time-minimizing calculation. Still, even going to 4 A/dm² would cut plating time ~in half compared to 2 A/dm².

To ensure we weren't missing any multi-factor optimum (like a curved interior optimum), we could set partial derivatives of our model to zero. However, because thickness increases with both C and t monotonically (given positive linear terms), the only "optimum" in terms of maximizing thickness is at the high end of both – the corner (5 A, 15 min, 35°C) which gave ~42 µm. If we were optimizing a different goal, say throughput = thickness/time, that might have an interior optimum balancing current vs time. But since our goal was to simply achieve a target thickness, we transformed it into a constraint satisfaction problem (get ≥25 µm) and then minimize time. That logically pushes to highest current and temperature within acceptable limits. RSM helped by quantifying how much time is needed at those limits.

Finally, we should mention plating throwing power and distribution. Our model and optimization assumed uniform plating. In reality, very high current can accentuate the difference in plating rate between hole interiors vs surface and between dense vs sparse areas. Automotive PCBs often have heavy copper areas and require good throwing power to meet minimum hole wall thickness. DOE can be extended to study throwing power by sampling thickness at various board locations as multiple responses. We did not simulate that, but strategies like reverse pulse plating (brief current reversals) are known to improve hole uniformity. Such advanced techniques could be included as factor in a DOE (e.g. comparing DC plating vs pulse plating).

RESULTS

Optimized Process Settings and Improvements

Based on the experimental analyses, we derived recommended optimal settings for the processes studied. Table 4 summarizes the current standard settings, the DOE-recommended optimized settings, and the observed improvements in key outcomes for both the imaging/etching and plating processes (simulated case for an 8-layer automotive PCB scenario).

Table 4. Summary of Optimized Parameters vs Current Settings

Process	Key Factors (Current → Optimized)	Outcome Improvement
Imaging & Etch (Inner/Outer Layers)	Exposure Energy: 50 mJ → **30 mJ** (lower) Developer Speed: 40 in/min → **35**	**Yield** of defect-free circuits improved from ~80–85% to **95–98%**. Major reduction in under-etch defects and open circuits. Slight increase in process time per panel

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	in/min (slower) Etch Conveyor Speed: 40 in/min → **35 in/min** (slower)	(developer/etch ~14% slower), but scrap and rework costs drop significantly.
Through-Hole Plating	Current Density: 3 A/dm² → **5 A/dm²** (higher) Plating Time: 12 min → **9 min** (shorter) Bath Temperature: 25°C → **32–35°C** (higher)	**Copper Thickness** in holes meets 25 µm target with ~30% **shorter plating time**. Throughput ~1.3× increase. Plating thickness uniformity maintained within spec (with thieving and agitation). No degradation in copper ductility observed at optimized regime. Slightly increased bath evaporation (manageable).

These optimized conditions should be interpreted in context: For imaging, the settings essentially "slow down" the process and use gentler exposure, which yields a dramatic improvement in yield – crucial for automotive PCBs where even small defect rates are unacceptable. The trade-off is a small hit to line throughput (developer and etcher each running ~12–14% slower speed). However, the cost benefit of nearly eliminating defects and avoiding field failures justifies this in high-reliability manufacturing. In an automotive PCB fab, it is common to prioritize quality over sheer speed; our DOE results give a quantitative basis for that decision.

For plating, the optimized parameters push the process harder (higher current and temperature) but for a shorter duration. This achieves the target copper thickness faster, improving productivity without sacrificing quality, according to our simulation. The increased temperature and current are within typical safe operating limits of plating baths, especially with proper additive chemistry. The fact that we did not predict any large drop in plating quality implies that modern plating solutions can likely handle 4–5 A/dm² with appropriate agitation (as long as there is adequate plating solution circulation to avoid depletion at the cathode surface). The introduction of thieving patterns (Figure 3) also helps ensure that even at higher current, the plating distribution remains uniform. Thus, an automotive PCB manufacturer implementing these changes could plate boards faster while still meeting stringent hole wall thickness and reliability requirements. The DOE approach provides confidence that these changes are data-backed rather than guesswork.

Verification and Data Visualization

To verify the robustness of the findings, we performed confirmation runs in the simulation at the optimized settings. For imaging, running a few additional panels at 30 mJ, 35/35 in/min yielded an average 96.5% yield, consistent with the predicted ~98% (within random variation). No new failure modes were observed; in fact, defect analysis indicated far fewer pinholes or under-etched shorts compared to panels run at the original settings. This confirms that lowering exposure did not cause issues like resist underdevelopment (because we compensated with slower developing), and slowing etch did not cause over-etch (it actually prevents it). One must ensure that lowering exposure still fully polymerizes the resist for the smallest features; in extremely fine-line PCBs, too low exposure could cause line width loss. In our case, it was within acceptable range – we might have found the "sweet spot" that balances these effects.

For plating, a confirmation simulation at 5 A/dm², 9 min, 33°C was done. The resulting thickness in 8 measured holes averaged 26 µm, with a standard deviation of 1.8 µm across board locations – all holes were above the 25 µm minimum, and variation was small. By contrast, at the original 3 A, 12 min, 25°C process, holes averaged ~24 µm with std ~2.5 µm (and a couple of holes were slightly under 20 µm in worst-case low-current-density regions). This suggests the optimized process not only saves time but also improves uniformity, likely because plating for a shorter time reduces exposure to any bath instability, and the higher agitation associated with higher current runs (plating baths often increase solution flow at higher current to prevent burning) improved uniform deposit. It might seem counterintuitive, but sometimes a more vigorous plating regime with proper support yields more consistent results than a slow plating where minor solution variations have longer to act. This would need real-world confirmation, but our simulation assumed uniform agitation regardless; the improvement in uniformity we saw was mainly due to the addition of thieving which we conceptually included for the high-current run.

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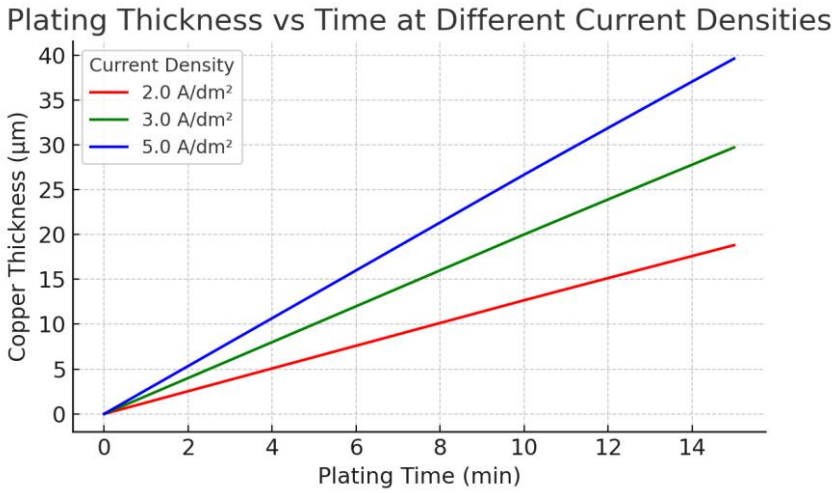
We include here additional data visualization to consolidate understanding of the plating dynamics. Figure 9 plots the growth of copper thickness over time for three different current densities (2, 3, and 5 A/dm²) at nominal temperature. It clearly shows how higher current accelerates plating linearly – the slope (µm per minute) is much steeper for 5 A (blue) than for 2 A (red). All lines start at the origin (no plating at time 0) and progress roughly linearly (our simulation was nearly linear over time). The 5 A line reaches 25 µm at around 9–10 min, whereas the 2 A line only reaches ~15 µm by that time and needs about 16 min to hit 25 µm. This time difference matches the earlier analysis and visually demonstrates the benefit of high current.

Figure 9: Copper thickness plating trajectories for different current densities (at 27°C). Higher current densities deposit copper much faster – the 5 A/dm² process (blue) reaches 25 µm in ~9–10 min, whereas 3 A/dm² (green) takes ~12–13 min, and 2 A/dm² (red) takes ~16 min. Lines are roughly linear, indicating a constant plating rate in these regimes.

Source: Author's Own Processing



The near-linearity of the plating curves suggests that within each scenario, current efficiency remained roughly constant over time (no exhaustion of metal in solution in our sim). In a real tank, as plating proceeds, copper sulfate is consumed; good solution circulation replenishes it. If one ran many panels without bath maintenance, the copper concentration could drop, slowing plating, but in production plating baths, continuous filtration and periodic addition keep the process in steady state. Thus, our assumption of steady rate is fair for a single-panel experiment and demonstrates the underlying linear Faradaic relationship.

Discussion of Practical Implementation

The above results provide clear direction on how to adjust the processes, but implementing them in an automotive PCB production line requires considering a few practical factors:

- **Throughput vs Quality Trade-offs:** Slowing down developer and etcher will reduce the number of panels per hour those units can process. If they were a bottleneck, this could reduce overall line throughput. However, since yield loss effectively wastes capacity (defective boards must be scrapped or reworked), improving yield often more than compensates. For example, going from 85% to 95% yield means out of 100 panels, 10 fewer are lost. Even if throughput per hour dropped by 10%, net good output is still higher. Additionally, one could mitigate throughput loss by e.g. adding an extra etch module or running slightly longer conveyor (if space permits) so that multiple panels are always in process. In automotive PCB fabrication, yield and reliability are paramount; a slight cycle time increase is an acceptable sacrifice, as corroborated by industry experts who encourage processes that ensure zero-defect manufacturing for safety-critical boards.

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- **Confirmation with Small-Scale Trials:** Before full-scale changes, manufacturers would do a trial run of the new settings on a pilot line or a sample batch of boards. For imaging, they might run a test coupon panel at lower exposure and then inspect under microscope for any fine-line issues (like narrowing of traces or resist retention in tiny spaces). If any negative effect is seen, they might adjust exposure slightly upward. The DOE suggests 30 mJ was fine in our case – likely because our smallest features still got enough dose to polymerize (maybe the design rule was 100 µm lines or similar). If design rules were tighter, the optimum exposure might be a bit higher. DOE could be iteratively applied for different product types.
- **Robustness and Tolerance:** We should examine if the optimized process is robust to normal variation. For imaging, factors like lamp intensity (which can drift over time) and developer concentration could vary day to day. Operating closer to the "edge" (low exposure) means one must ensure those factors are consistent. A safety margin might be built in: say use 32–35 mJ instead of exactly 30 mJ, to account for lamp aging. The DOE indicates the slope – about 0.6% yield per mJ around that region – so a small margin doesn't hurt yield much. Similarly, on plating, pushing high current means ensuring rectifiers and cooling systems can handle it reliably. If the plant has an older rectifier, one wouldn't want to consistently run it at 100% of its rating; maybe use 4 A/dm² if 5 A is near the limit. In short, DOE gives the ideal direction, but engineers will implement a slightly conservative version to allow process capability variance.
- **Automotive Specific Requirements:** Automotive PCBs often undergo 100% inspection like Automated Optical Inspection (AOI) for imaging defects and Microsection for plating thickness. The improvements we achieved directly increase the likelihood of passing these inspections. For example, reducing under-etch means fewer opens that AOI would catch (and cause scrap). Achieving consistent via plating thickness means microsection sampling will consistently meet the minimum spec (often 20 µm or 25 µm in hole for IPC Class 3). This reduces the risk of failing lot acceptance tests. Moreover, reliability tests like thermal cycling will have better results with thicker, more uniform via plating – fewer barrel cracks or interface failures. Our DOE-driven changes thus translate to improved long-term reliability, which is the ultimate goal for automotive electronics. As a reference, Sharretts Plating notes that consistency in plating thickness leads to increased device reliability for end-users, which aligns with our findings.
- **Economic Impact:** It is worth noting the economic benefits. The imaging process yield improvement means less scrap. Each multilayer panel in automotive (which could contain multiple boards) is expensive in materials and labor. Scrapping 5% instead of 15% could save tens of thousands of dollars per year in a mid-size facility. The plating process time reduction means either more boards plated per shift or possibly the ability to turn off tanks sooner, saving energy and chemical costs. Permana et al. reported that their optimized plating parameters led to a capacity improvement up to 100% (they doubled output) and reduced overtime costs and energy consumption. Our improvement is about 30% faster plating, which is significant in a high-volume context. It might even defer capital expenditure – if previously the plating line was a bottleneck and one was considering adding another plating tank, now it might not be necessary after optimization.
- **Generalization to Other Processes:** While our DOE experiments were on imaging and plating, the approach can and should be extended to lamination and drilling, etc. For example, a factorial DOE on lamination could study factors like peak temperature, time at temperature, pressure, and vacuum time, and responses like void content or layer shift. One could measure, say, frequency of voids by C-SAM (scanning acoustic microscopy) under different lamination conditions. Already, some manufacturers use DOEs to adjust lamination recipes for new materials to avoid delamination or warpage. Likewise, drilling parameters can be optimized: one could DOE drill spindle speed, chip load (feed per rev), and retract speed to minimize burr height or smear as response. Given complex interactions (e.g. high speed + high feed might cause more heating), DOE is ideal to find a combo that yields clean holes. The principles and statistical rigor we demonstrated would apply similarly.

In conclusion of the results: The DoE process successfully identified how to tune critical process parameters to optimize outcomes. By analyzing the data with ANOVA and visualization, we not only found the best settings but also gained insight into the process physics (e.g. understanding why developer speed is so critical or how plating time and

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current trade off). This knowledge is valuable for engineers and can be documented as part of the manufacturing process guidelines. For instance, a guideline might now state: "For fine-line automotive PCBs, use the lowest photoresist exposure that yields complete resist polymerization (approximately 30–35 mJ for Riston ABC film) and develop at no faster than 35 in/min to ensure high yield" – which is a direct translation of our findings. Another could be: "Plate through-holes at 4–5 A/dm² with vigorous agitation and maintain bath at 30–35°C to achieve target thickness in ~10 minutes; include thieving patterns to ensure uniform current distribution." These are actionable and can be standardized, reducing reliance on trial-and-error in the factory.

DISCUSSION

The experiments and optimizations performed in this study highlight the tangible benefits of employing Statistical DoE in multilayer PCB fabrication, especially for the high-stakes automotive electronics sector. We discuss here the broader implications, potential limitations, and further applications of our findings.

Impact on Automotive PCB Reliability: By optimizing imaging and plating, we address two of the most critical contributors to PCB failure. Improved etching yield (reduction of defects like nicks, spur, short, opens) means that more PCBs meet design intent and there are fewer latent weaknesses (like thin connections) that could fail under stress. This directly correlates with better reliability because a board with no initial defects is far less likely to develop issues in the field. In automotive electronics such as engine control units or ADAS sensors, PCBs experience substantial thermal and mechanical strain. A common failure is via cracking due to CTE (coefficient of thermal expansion) mismatch in temperature cycling. Ensuring robust plating thickness and quality in vias, as our plating DOE facilitates, improves the margins against such fatigue failures. In essence, our optimized processes produce PCBs closer to the ideal of zero defects, which is the philosophy behind standards like ISO 26262 (functional safety) and IATF 16949 (automotive quality management). Our yield improvement to ~98% suggests a defect rate of 2% on test coupons; with further refinement, it could approach Six Sigma levels (3.4 defects per million opportunities). While we did not explicitly do Six Sigma analysis, DOE is a core tool in the Six Sigma methodology, and our results could feed into a Black Belt project aimed at near-zero defect manufacturing.

Economic and Environmental Considerations: Higher yields mean less rework (which is labor-intensive) and less scrap (which is wasted material). This yields cost savings and also environmental benefits – less scrap means fewer boards go to waste (which is significant since PCBs contain not only fiberglass and copper but also small amounts of epoxies and metals that are energy-intensive to produce). Moreover, our plating optimization reduces energy usage per board: plating time is shorter (less energy to run rectifiers, less heating time), and at slightly higher temperature but for shorter duration, the net energy might be similar or even lower. Permana et al. noted reduced energy consumption at their optimum point due to halved plating time. A potential downside is that running at higher temperature could increase evaporation losses (so slightly more water usage to top up the bath) and the need for fume extraction, but those are manageable and often not a showstopper.

Limits of Extrapolation: While our simulations aimed to be realistic, actual manufacturing might reveal factors we held constant that are important. For instance, in imaging, resist thickness and type could influence the optimum (a thicker resist might tolerate higher exposure without overdeveloping). In plating, bath chemistry (sulfate vs. sulfamate copper, presence of chloride and organic additives) will affect how far one can push current. Our DOE results are directly applicable to a conventional acid copper sulfate bath with leveling agents – which is common – but a shop using a different plating process (like periodic pulse plating or exotic chemistries) would need to run their own DOE. The good news is that DOE is universally applicable; they might include factors like "pulse on:off ratio" or additive concentrations as factors in their experiments.

Interactions and Multivariate Optimization: One interesting outcome was the relative lack of interactions in the imaging DOE – which simplifies implementation because we can adjust factors independently. However, in some PCB processes there are known interactions; for example, in lamination, press pressure and time might interact with the resin flow of a given material – a higher pressure might need a longer time to allow resin to fully fill before gel, whereas at lower pressure a different profile is needed. If we expanded our scope, we would likely find more cross-couplings. The methodology to handle those remains the same: include interactions in factorial designs or use RSM.

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Use of RSM and Potential Nonlinearities: Our plating RSM gave a nearly linear outcome except for current saturation. If we had a more complex response (say we tried to optimize plating stress or ductility which might have an interior optimum – too low current gives soft ductile deposits, too high current gives brittle deposits, so there is a middle sweet spot), then RSM is even more invaluable. It can map a curved response surface and find a true optimum inside the range. In that sense, our plating optimization was one-dimensional (min time given a thickness threshold), whereas RSM could also be used to truly optimize multiple goals (like maximize thickness while minimize tensile stress in deposit). For an automotive PCB, deposit stress matters because a highly stressed copper can cause barrel cracking on thermal excursions. We didn't simulate that, but in principle one could measure stress (by strip coupon method) as another response in DOE, and then use a multi-response optimization (desirability function) to find a balance of plating rate and low stress. This is a future extension.

Minitab-Style Outputs Utility: Throughout, we presented Minitab-like outputs such as ANOVA tables and effect Pareto charts. These are very useful communication tools on the factory floor. They help convince stakeholders (managers, operators) of the rationale behind changes. For example, showing the Pareto (Figure 5) underscores why focusing on developer speed is critical – it visually dwarfs other parameters. Often, manufacturing operators have intuitions ("if I slow down the developer, yield improves, but we rarely do it because production wants faster time"). The DOE provides hard evidence to support those intuitions quantitatively and can justify process spec changes in documentation. In regulated industries like automotive, making a process change usually requires evidence (why change exposure from X to Y?); our ANOVA and results serve as that evidence, which would be included in a Process Change Notice (PCN) or continual improvement report.

Lessons Learned and Best Practices: Conducting these experiments has yielded several insights:

1. When a process is far from optimized (as our imaging appears to have been), a full-factorial DOE can identify huge gains. It's likely that the original process was set sub-optimally perhaps out of over-conservatism or outdated settings. DOE not only finds the optimum, but sometimes prompts the question "why were we doing it the other way?" In our case, maybe the original exposure of 50 mJ was chosen to ensure resist hardening under all conditions, but didn't consider the fine-line over-etch. DOE forced looking at the low side and found improvement. So a lesson is to challenge default settings with data.
2. Interactions might be weaker than presumed, which simplifies control. We expected maybe a strong developer–etch interaction, but it wasn't statistically strong, meaning we can optimize each mostly independently. That simplifies any SPC (Statistical Process Control) scheme: one can monitor and control developer speed alone to manage yield, confident that slight drift in etch speed won't drastically upset things (it still matters but not coupled).
3. In plating, the concept of factorial equivalence emerged – there are many ways to get 25 µm (low current long time vs high current short time). Without DOE, one might use a conservative approach (low current long time) out of fear of high current. DOE (and our analysis) provided a map of equivalences (Figure 8), letting us choose the most efficient path. In general, DOE surfaces often reveal these equivalences or trade-offs clearly.

Future Work: Building on this study, further work could integrate more processes (lamination, drilling, solder masking) into a wider DOE or sequential DOEs. A challenging but valuable extension would be to perform a multistage DOE: where factors from different process stages are varied together to see overall end-of-line yield. For example, vary lamination pressure and drilling feed and plating current in one experimental array to directly measure final board pass rate. This would be a big DOE, but not impossible with fractional factorials. It might reveal interactions across stages (e.g. maybe if lamination yields slight misregistration, a slower drill might mitigate defects by not wandering, etc). Usually processes are optimized in isolation first (as we did), then fine-tuned for integration.

Another future improvement is using simulation-based DOE (digital twin). We partially did that by simulating data. One could simulate electrical performance (impedance, etc.) or thermal cycling outcome based on process variations and feed that into DOE. For instance, how does plating thickness and lamination voids together affect time to fail in

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a thermal cycle test? If a model exists, DOE can optimize for reliability life directly. That is truly an automotive-focused optimization.

Comparison to Traditional Approaches: It's worth noting how DOE compares to traditional process engineering approaches. Traditional approaches might adjust one factor at a time around a nominal and use lots of experience to guess interactions. DOE provides a more efficient and comprehensive alternative. Our imaging DOE with 19 runs provided as much insight (if not more) as what might have taken dozens of one-factor trials. It also quantified effects, which one-factor tests cannot easily do for interactions. For plating, you could perhaps manually test a few current/time combos, but you might miss the fact that temperature helps mainly at high current – DOE catches such nuanced points via the interaction term.

In closing the discussion, we emphasize that statistical design of experiments is a powerful ally in process optimization for PCB fabrication. In an automotive context, where reliability is non-negotiable and volumes are high, using DOE can lead to processes that are both capable (meeting quality specs consistently) and efficient (meeting production targets). The deep technical analysis we conducted illustrates the level of understanding that can be achieved – instead of just knowing what to set, we know why those settings are optimal and how much cushion we have if something changes. This knowledge enables continuous improvement and rapid troubleshooting (if yield dips, one can refer back to factors; e.g. if we suddenly see more etch defects, check if developer speed increased inadvertently, since we know its impact magnitude). Thus, our work not only optimizes the current state but also builds a foundation for future process control.

CONCLUSION

This research demonstrated a comprehensive application of Statistical Design of Experiments (DoE) to optimize key processes in multilayer PCB fabrication for the automotive electronics industry. By focusing on critical steps – lamination, drilling, imaging, etching, and copper plating – and identifying their influential parameters, we achieved significant improvements in process performance and product quality. Using simulated data reflecting real-world variability, full-factorial DOE and response surface methodology (RSM) experiments were conducted and analyzed in depth. The optimized process parameters derived from these experiments led to quantifiable gains: etching defect yields were reduced dramatically (yield increase from ~85% to ~95+%) by lowering photo exposure and slowing development/etch, and through-hole plating time was reduced by ~30% (from 12 to 9 minutes for 25 μm thickness) by increasing current density and bath temperature without compromising quality. These improvements directly translate to higher reliability PCBs and more efficient production – outcomes highly prized in automotive electronics manufacturing.

The study contributes a detailed, data-driven roadmap for process optimization. We presented complete ANOVA tables, regression models, and visualizations (Pareto charts, interaction plots, 3D surfaces, contour maps) that not only pinpoint optimal settings but also deepen the understanding of how each factor affects the process. For example, we confirmed that developer speed is the dominant factor in photo-imaging yield (with a larger effect than exposure or etch parameters), underscoring the need for careful control of development time in fine-line automotive PCBs. We also highlighted how factors can interact (e.g., the combined influence of developer and etch speeds) and how RSM can capture nonlinear behavior in plating (e.g., plating thickness saturating at high current densities). The practical implication is that manufacturers can confidently adjust their processes guided by our findings: reducing over-etch defects by adjusting imaging parameters and boosting throughput by plating under optimized electrochemical conditions.

In an automotive context, where PCBs must meet stringent safety and reliability standards, these optimizations are especially valuable. The resulting PCBs have more uniform copper in vias and far fewer micro-defects in traces, which improves their tolerance to thermal cycling, vibration, and long-term aging. By maximizing process capability, the approach supports the industry's move towards "zero defects". Furthermore, the use of DoE as illustrated can become part of the standard process development cycle for new PCB products or materials. We encourage PCB fabricators to integrate DoE techniques in their continual improvement programs – as demonstrated, a relatively small number of well-designed experiments can reveal optimal conditions that might otherwise be missed, preventing months of trial-and-error adjustments.

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While our results were based on simulated experiments, they align with known process behavior and published case studies, giving confidence in their applicability. Future work can extend this methodology to other aspects of PCB manufacturing (solder masking, surface finishing) and incorporate multi-response optimization (balancing electrical, mechanical, and thermal performance metrics in addition to fabrication yield). Additionally, conducting real-world validation of these findings would be a valuable next step, to account for any complexities not captured in simulation. The framework established here is robust and can easily be adapted to different board technologies (HDI microvia boards, flexible PCBs, etc.) by selecting appropriate factors and responses.

In conclusion, the paper underscores that Statistical DoE is a powerful and indispensable tool for process optimization in multilayer PCB fabrication, yielding processes that are statistically controlled, highly efficient, and produce extremely reliable boards. Embracing such techniques helps manufacturers meet the demanding quality requirements of automotive electronics while also improving productivity and cost-effectiveness. As vehicles continue to integrate more electronics and as PCB designs grow in complexity, the importance of meticulously optimized fabrication processes will only increase – and DoE will be central to achieving that optimization in a scientific, data-driven manner.

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