

Comparative Analysis of Triangle and Trapezoidal Carrier Signal for 3-Level ANPC Inverter

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ABSTRACT

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Introduction: Multilevel topologies are becoming more and more popular, and new topologies have been created. High voltage is used to create staircase output in order to lower the THD. For the carrier signal triangle and trapezoidal signal has been arranged in Phase opposition pulse width modulation (PODPWM), phase disposition pulse width modulation (PDPWM), alternative phase opposition disposition pulse width modulation (APODPWM), phase shifted PWM (PSPWM), to analyze the total harmonic distortion for ANPC topology. In this paper the RMS value of phase voltage and THD value of output voltage is comparing and the most effective PWM technique for a 1500V DC bus, three phases, 3 level ANPC inverter is identified for use with 1200V switching devices. SIN wave is used as a reference signal to simulate and compare two different carrier signals for three-level inverter in PSIM software.

Objectives: Several innovative modulation techniques for ANPC are incorporated into the control algorithm. The optimization targets can be divided into the following three categories.

- The main objective is to Reducing the voltage THD.
- The second objective is to increase the output voltage by recommending suitable modulation techniques.

Keywords: PODPWM, PDPWM, APODPWM, Trapezoidal triangle signal, ANPC inverter

INTRODUCTION

For a 3 level multilevel inverter various topologies are used but ANPC topology for a single DC source becoming more and more popular. High voltage is used to create staircase output in order to lower the THD. Phase opposition pulse width modulation (PODPWM), phase disposition pulse width modulation (PDPWM), alternative phase opposition disposition pulse width modulation (APODPWM), phase shifted PWM (PSPWM) are some of the PWM techniques used to analyze the total harmonic distortion for ANPC topology.[1-3] In this paper the RMS value of phase voltage and THD values are analysed by using the most effective PWM technique for a 1500V DC bus, three phases, three level ANPC inverter is identified for use with 1200V switching devices. SIN-Triangle/Trapezoidal PWM techniques have been used in PSIM to simulate a three-level inverter.

OBJECTIVES

The ANPC topology first proposed by ABB. Figure 1 depicts the structure of a three-level ANPC (3L-ANPC) that uses switching devices in place of the clamp diodes in a three-level NPC topology.

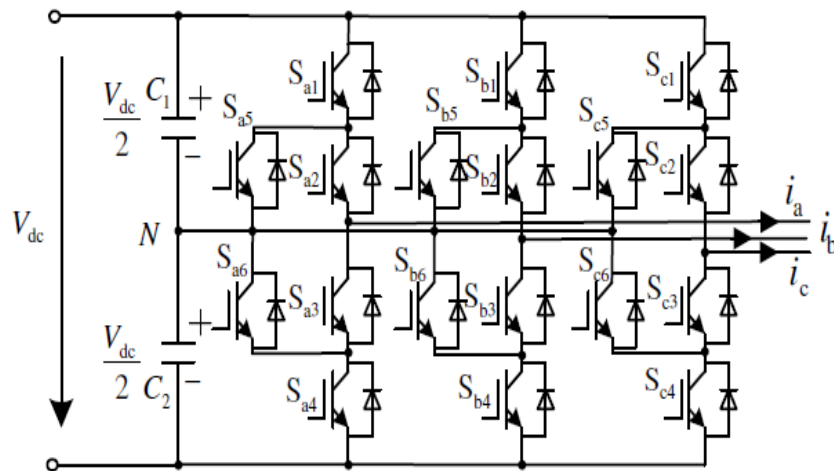


Figure 1. Topology for 3 level ANPC inverter

Several innovative modulation techniques for ANPC are incorporated into the control algorithm. The optimization targets can be divided into the following three categories. In this paper the stray inductance also included in the simulation as the DC bus voltage is at 1500V, the due to stray inductance at the switching instant high voltage spike also to be appear at the switching device.[4-5]

- The main objective is to Reducing the voltage THD.
- The second objective is to increase the output voltage by recommending suitable modulation techniques.

METHODS

The power quality issues mentioned in given reference paper has to be mitigates. For the 3 level ANPC inverter there are 48 switching states are available, some of the switching states are dangerous and can cause the short circuit of the DC bus voltage.[6-8,10] When the switch S5 and/or S6 are in ON condition some of the switching states are no longer dangerous. All the switches operate in different combination to generate three level output voltage. Depending upon the switching time the switches may operate in either high frequency mode (HF) or operate on output low frequency (LF), the basic principle is describing in references. “Figure 2” shows the PWM method based on HF/LF combination is describes. The zero state, in which the current travels via various conduction pathways, is where the PWM techniques diverge from one another.[9,11]

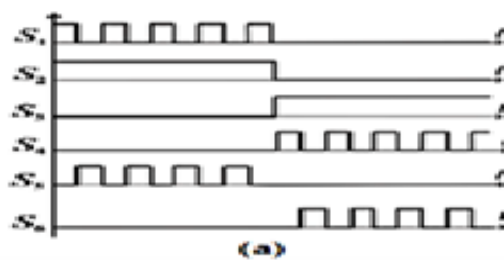


Figure 2 PWM methods for ANPC inverter

This PWM method has an advantage by using it in ANPC application is that it reduce the stray inductance from a long commutation loop to the short commutation loop. In this PWM method has a switching device S2 and S3 having a stat transition at power frequency and hence the overall switching losses are less but the conduction losses are more. the proposed PWM method is is shown in “Figure 2”.[12]

To obtain the above PWM pulses SIN-Triangle/trapezoidal comparison method is more prefereble than the other techniques. [13-15]Unlike other optimized PWM methods, these methods have no need for look-up tables for the

desired switching states of power switches, extensive offline computations, or optimization techniques. Based on the phase arrangement triangle signals are arranged in Phase disposition PWM (PDPWM), Phase opposition disposition PWM (PODPWM), Alternative Phase Opposition Disposition PWM (APODPWM) as shown in “Figure 4”. [17-18]

The reference signal the mathematical expression is given in “Eq 1”

$$V_r = \sin(\omega^*t), V_y = \sin(\omega^*t - 2\pi/3), V_b = \sin(\omega^*t + 2\pi/3) \quad [1]$$

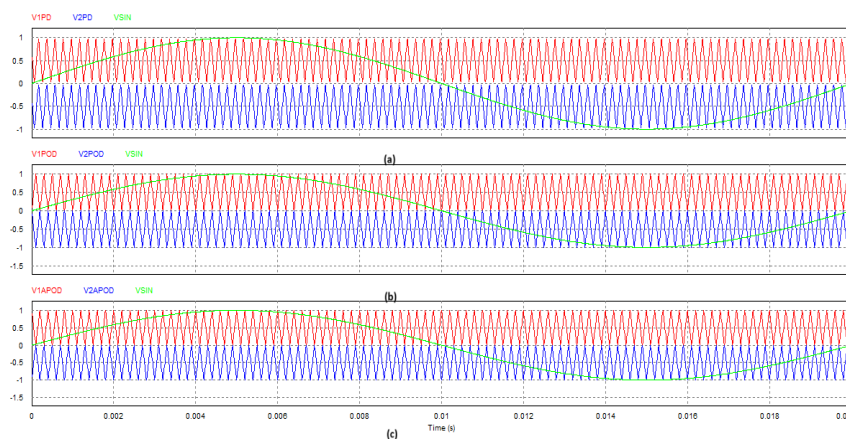


Figure 3. Phase arrangement of Triangle Carrier based PWM method for ANPC inverter (a) PDPWM (b) PODPWM (c) APODPWM

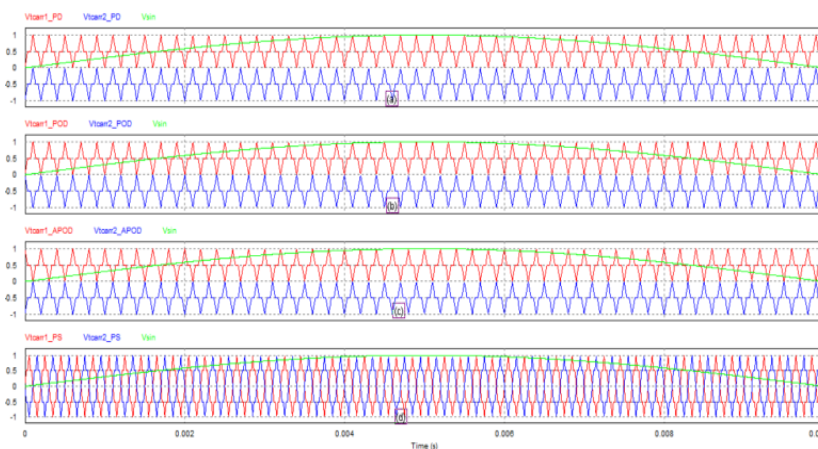


Figure 4. Different Trapezoidal Triangle Carrier based PWM method for ANPC inverter (a) PDPWM (b) PODPWM (c) APODPWM (d) PSPWM

SIMULATION OF 3 LEVEL ANPC INVERTER

The following parameters are used to run the simulation in this paper. The following is the selection of the simulation parameters.

$L_{load} = 2400\mu H$, $L_q = 30nH$, $L_{qclamp} = 120nH$, $L_{qinv} = 120nH$, $L_{bus} = 120nH$, $V_{dc} = 1500V$, $C_1 = 28.2mF$, $C_2 = 28.2mF$, $R_{load} = 27m\Omega$. 5 kHz is the switching frequency (f_{switch}). The choice for a switching device is 1200V IGBT. The modulation index is taken as 1 and measures the THD value of output phase voltage and the peak voltage across each switching devices.

A triangle wave with various phase combinations in PDPWM, PODPWM, PSPWM and APODPWM techniques can be used to generate the PWM pulses carrier wave. The resulting wave can then be compared to the reference wave produced by various techniques.

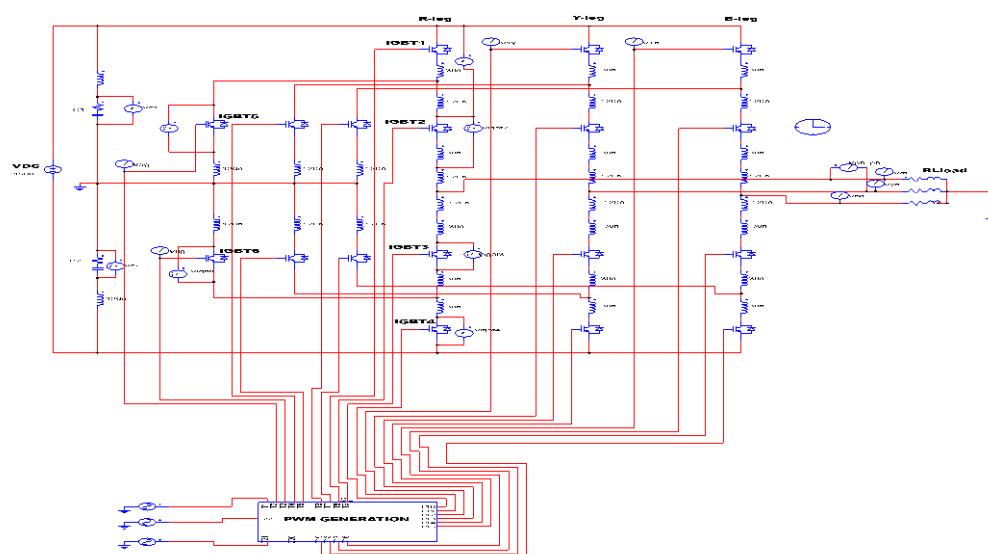


Figure 5 Simulation schematic diagram of ANPC inverter

RESULTS

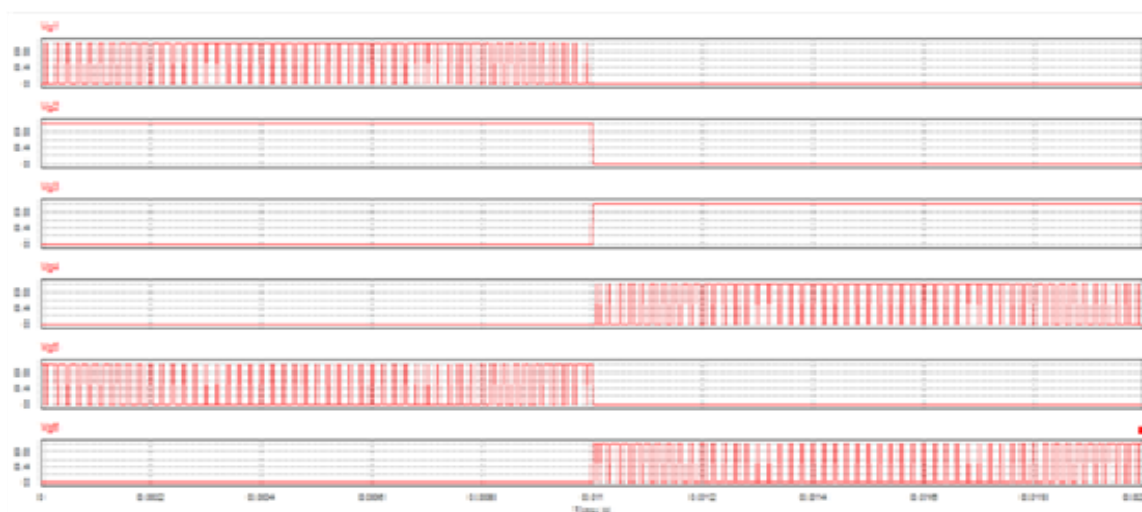


Figure 6 ANPC inverter gate signals for switch Sa1 to Sa6

Table 1 Comparison of output RMS voltage, output voltage THD and Peak voltage across each switching device

Method	RMS value of phase voltage V_{rb}	THD	Peak voltage across each IGBT					
			S1	S2	S3	S4	S5	S6
PDPWM with triangle signal	966	35.61%	796	795	783	827	784	795
PODPWM with triangle signal	987	41.02	1047	916	828	892	828	916
APODPWM with triangle signal	984	41.89%	874	799	783	817	785	799
PSPWM with triangle signal	1109	40.04%	832	790	787	826	787	790
PDPWM with trapezoidal signal	992	32.63%	887	878	870	909	871	879
PODPWM with trapezoidal signal	989	33.91%	794	792	791	804	791	792
APODPWM with trapezoidal signal	1007	39.68%	854	804	790	804	791	804
PSPWM with trapezoidal signal	1117	35.40%	854	805	798	864	798	805

DISCUSSION

The carrier signal are formed by trapezoidal and triangle waveshape and its compared with Sinusoidal reference signal to generate the different gate pulses for the switches. Different phase combinations for carrier signal are compared and results shown in “Table 1”. The highest RMS voltage 1117 V is obtained when PSPWM method in trapezoidal triangle but the THD value is higher. The lowest THD value 32.63% is obtained when PDPWM method is used in trapezoidal triangle. In all the methods across the switching device the peak value obtained is less than 1200V.

REFERENCES

- [1] Agarwal, A., & Agarwal, V. (2012). FPGA realization of trapezoidal PWM for generalized frequency converter. *IEEE Transactions on Industrial Informatics*, 8(3), 501–510. <https://doi.org/10.1109/TII.2012.2193406>
- [2] Alam, M. A., Islam, M. T., Rahman, M. F., Ahmed, A., Ur Rahman, M. N., & Hossain Maruf, M. N. (2024, January 18). Power inverter performance with trapezoidal triangular carrier and triangular based SPWM technique: A comparative analysis. In *2024 Third International Conference on Power, Control and Computing Technologies (ICPC2T)* (pp. 374–379). Raipur, India. <https://doi.org/10.1109/icpc2t60072.2024.10475019>
- [3] Altun, M., Tur, M. R., & Cakmak, F. (2022). 24V Input 12V and 36V Output Buck-Boost Converter design. *2nd Advanced Engineering Days*, 90–92.
- [4] Bruckner, T., Bernet, S., & Guldner, H. (2005). The active NPC converter and its loss-balancing control. *IEEE Transactions on Industrial Electronics*, 52(3), 855–868. <https://doi.org/10.1109/TIE.2005.847586>
- [5] Chen, H., Ai, S., Nie, Z., Cui, F., & Yuan, P. (2023). Modulation strategy for suppressing peak voltage spikes of SiC-MOSFETs during ANPC commutation. *IEEE Access*, 11, 27631–27640. <https://doi.org/10.1109/ACCESS.2023.3245817>
- [6] Anjaneya Vara Prasad, P., & Dhanamjayulu, C. (2023). An overview on multi-level inverter topologies for grid-tied PV system. *International Transactions on Electrical Energy Systems*, 2023, 1–55. <https://doi.org/10.1155/2023/9690344>
- [7] Binojkumar, A. C., & Narayanan, G. (2014, December). Variable switching frequency PWM technique for induction motor drive to spread acoustic noise spectrum with reduced current ripple. In *Proceedings of the 2014 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. Mumbai, India. <https://doi.org/10.1109/PEDES.2014.7042071>
- [8] Biswas, A. (2016, December). Study of trapezoidal PWM on a 1 ϕ AC-AC frequency converter. In *Proceedings of the 2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*. Trivandrum, India. <https://doi.org/10.1109/PEDES.2016.7914315>
- [9] Chen, H., Ai, S., Nie, Z., Cui, F., & Yuan, P. (2023). Modulation strategy for suppressing peak voltage spikes of SiC-MOSFETs during ANPC commutation. *IEEE Access*, 11, 27631–27640. <https://doi.org/10.1109/ACCESS.2023.3245817>
- [10] Dhasharatha Varma, N. R., Spandana, A., Kumar, P. A., Venumadhav, B., & Kumar, B. P. (2023, April 11). Design and implementation of three-phase three-level NPC inverter. In *2023 7th International Conference on Trends in Electronics and Informatics (ICOEI)* (pp. 106–110). Tirunelveli, India. <https://doi.org/10.1109/ICOEI56765.2023.10125979>
- [11] Florica, D., Florica, E., & Gateau, G. (2008, November). Three-level active NPC converter: PWM strategies and loss distribution. In *2008 34th Annual Conference of IEEE Industrial Electronics*. Orlando, FL. <https://doi.org/10.1109/IECON.2008.4758494>
- [12] Franquelo, L., Rodriguez, J., Leon, J., Kouro, S., Portillo, R., & Prats, M. (2008). The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine*, 2(2), 28–39. <https://doi.org/10.1109/MIE.2008.923519>
- [13] Gui, H., Chen, R., Zhang, Z., Niu, J., Ren, R., Liu, B., & Choi, B. B. (2020). Modeling and mitigation of multiloops related device overvoltage in three-level active neutral point clamped converter. *IEEE Transactions on Power Electronics*, 35(8), 7947–7959. <https://doi.org/10.1109/TPEL.2019.2962621>
- [14] Gülbudak, O., & Gökdağ, M. (2022). Performance evaluation of model predictive control method for neutral point clamped inverter. *Turkish Journal of Engineering*, 6(3), 245–250. <https://doi.org/10.31127/tuje.962857>

- [15] Haq, S., Biswas, S. P., Hosain, M. K., Rahman, M. A., Islam, M. R., & Jahan, S. (2021). A modular multilevel converter with an advanced PWM control technique for grid-tied photovoltaic system. *Energies*, *14*(2), 331. <https://doi.org/10.3390/en14020331>
- [16] Hassan, J., Minambres-Marcos, V., Barrero-Gonzalez, F., Alvi, A. A., Malinowski, M., & Martinez-Caballero, L. (2023, September 4). A comparative study of three-phase inverter topologies for common mode voltage reduction in photovoltaic applications. In 2023 25th European Conference on Power Electronics and Applications (EPE'23 ECCE Europe). Aalborg, Denmark. <https://doi.org/10.23919/EPE23ECCEurope58414.2023.10264522>
- [17] Inzunza, R., Okuyama, R., Tanaka, T., & Kinoshita, M. (2015, November). Development of a 1500Vdc photovoltaic inverter for utility-scale PV power plants. In 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEEC). Taipei, Taiwan. <https://doi.org/10.1109/IFEEEC.2015.7361615>
- [18] Jamal, I., Elmorshedy, M. F., Dabour, S. M., Rashad, E. M., Xu, W., & Almakhlles, D. J. (2022). A comprehensive review of grid-connected PV systems based on impedance source inverter. *IEEE Access*, *10*, 89101–89123. <https://doi.org/10.1109/ACCESS.2022.3200681>