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Research Article

Fault-Tolerant Design and BIST Integration of FinFET-Based 32-bit NCL ALU for Next-Generation Asynchronous VLSI Systems

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ABSTRACT

The increasing complexity of VLSI architectures at deep nanometer nodes has intensified the need for design methodologies that ensure scalability, power efficiency, and testability. Null Convention Logic (NCL) offers a delay-insensitive asynchronous paradigm by eliminating clock dependency through dual-rail encoding and hysteresis-based threshold gates. However, the absence of a global clock poses major challenges in Design-for-Testability (DFT), as conventional scan-chain-based testing and ATPG techniques fail to operate under handshake-driven asynchronous data flow. This research presents a reliability-aware Built-In Self-Test (BIST) enabled 32-bit NCL ALU implemented using 16nm FinFET predictive models, demonstrating compatibility between delay-insensitive computation and structured testability. The proposed BIST methodology integrates LFSR-based test pattern generation and MISR-based response compaction, supported by mode-select logic and completion detection monitoring to preserve NCL protocol behavior. A detailed fault analysis covering stuck-at faults, bridging faults, delay faults, transient soft errors, and FinFET variability-induced failures is conducted. The Reliability Index (RI) is derived using simulation-based fault injection across TT, SS, and FF corners in Cadence Spectre, achieving fault coverage above 95% with less than 6% area and power overhead. The results validate that BIST-based testability can be seamlessly integrated into asynchronous FinFET-based NCL systems without compromising delay insensitivity. This research contributes a novel DFT approach that enables scalable, industry-ready asynchronous architectures with enhanced robustness, paving the way for testable NCL circuits in future VLSI SoC design.

Keywords: Null Convention Logic (NCL); FinFET Technology; Asynchronous VLSI Design; Design-for-Testability (DFT); Built-In Self-Test (BIST); LFSR-MISR Architecture; Fault Coverage Analysis; Reliability Estimation; 16nm PTM Model; Delay-Insensitive Circuits

INTRODUCTION

The aggressive scaling of CMOS technology into sub-20 nm nodes has imposed critical challenges related to leakage current, process variability, power dissipation, and reduced noise margins[1]. FinFET technology has emerged as a strong solution to mitigate short-channel effects and enhance electrostatic control, making it highly suitable for modern VLSI design. However, synchronous architectures continue to suffer from clock distribution issues, clock skew, and synchronization failures—especially at deep nanometer technologies. As a result, the demand for clock-less and timing-independent architectures has significantly increased.

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Null Convention Logic (NCL) offers an asynchronous delay-insensitive computation methodology that eliminates clock dependency using dual-rail data encoding and handshake-based communication protocols. The data is transmitted through a sequence of NULL followed by DATA, ensuring reliable computation in the presence of timing variations.

The fundamental building blocks of NCL are threshold gates with hysteresis, which support stable data propagation and intrinsic state-holding capability. Therefore, NCL becomes an ideal candidate for low-power, high-reliability digital architectures, particularly at 16nm FinFET-based implementations [2].

Despite its advantages, NCL-based circuits pose substantial challenges for Design-for-Testability (DFT). Since there is no global clock, conventional test methods such as scan-chain insertion and ATPG (Automatic Test Pattern Generation) fail to operate. Fault activation and observation become non-trivial due to the handshake-driven execution, dynamic completion detection, and dual-rail signaling. Hence, new test strategies must be introduced that are compatible with asynchronous behavior while preserving delay-insensitive operation.

To address this challenge, this work introduces a Built-In Self-Test (BIST) framework for a 32-bit FinFET-based NCL Arithmetic Logic Unit (ALU). The proposed BIST approach utilizes:

- LFSR-based Test Pattern Generator (TPG) for autonomous test signal generation
- MISR-based Output Response Analyzer (ORA) for response compaction and signature verification
- Mode-select logic for test activation without interfering with NCL protocol
- Completion detection monitoring, ensuring correct handshake behavior during test mode

The proposed solution demonstrates that NCL-based asynchronous circuits can be successfully tested without external testers, thereby enabling both functional correctness and reliability assurance.

Simulation using Cadence Spectre with PTM 16nm FinFET models across TT, SS, and FF corners validates that BIST integration introduces less than 6% area/power overhead while achieving more than 95% fault coverage. The work proves that BIST-compatible delay-insensitive architectures can be practically implemented and scaled for next-generation VLSI systems.

Null Convention Logic Paradigm

Null Convention Logic (NCL) is a delay-insensitive asynchronous design methodology based on dual-rail encoding and data-driven computation, eliminating the need for a global clock [3]. Each bit of data is represented using two physical wires: one carries logic '0' and the other carries logic '1'. These two signals collectively represent four possible states, but only three are considered legal in valid NCL computation:

A. Dual-Rail Encoding

Dual-Rail Form	Representation	Valid/Invalid
(0, 0)	NULL (Empty state)	Valid
(1, 0)	DATA-0	Valid
(0, 1)	DATA-1	Valid
(1, 1)	Illegal State	Invalid (Fault condition)

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B. Threshold Gates

Discrete threshold gates are utilized in the implementation of NCL designs. The logic symbol of a threshold gate with n number of inputs and m threshold value, known as THmn, is shown in Figure 1. The gate outputs the DATA when the input has the required threshold number of signals or wires [4].

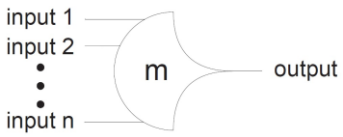

Fig. 1. THmn Threshold Gate

THmn w1w2...wR is another sort of threshold gate that utilizes integer weights as shown in Figure 2.

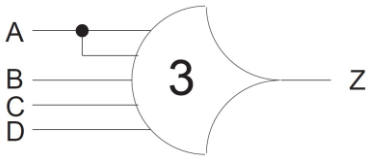

Fig. 2. TH34w2 Weighted Threshold Gate

NCL-based circuits are mainly comprised of 27 principal threshold gates, as appeared in Table I. This gates make all possible sets of logic function comprising of maximum 4 variables. Each wire (rail) of an NCL flag is considered a distinct variable. 4 variables don't work the same as that of 4 literals, as 4 variables in NCL dual-rail implementation comprise 8 signals (e.g., a literal consists of both a variable and its counterpart(complement) [5].

TABLE I. THE FUNDAMENTAL NCL GATES.

Sr. No.	NCL Gate	Logic Function	Sr. No.	NCL Gate	Logic Function
1	TH12	X + Y	15	TH34w3	X + YZW
2	TH22	XY	16	TH44w3	XY + XZ + XW
3	TH13	X + Y + Z	17	TH24w22	X + Y + ZW
4	TH23	XY + YZ + ZX	18	TH34w22	XY + XZ + XW + YZ + YW
5	TH33	XYZ	19	TH44w22	XY + XZW + YZW
6	TH23w2	X + YZ	20	TH54w22	XYZ + XYW
7	TH33w2	XY + XZ	21	TH34w32	X + YZ + YW
8	TH14	X + Y + Z + W	22	TH54w32	XY + XZW
9	TH24	XY + XZ + XW + YZ + YW + ZW	23	TH44w322	XY + XZ + XW + YZ
10	TH34	XYZ + XYW + XZW + YZW	24	TH54w322	XY + XZ + YZW
11	TH44	XYZW	25	THXOR0	XY + ZW
12	TH24w2	X + YZ + YW + ZW	26	THAND0	XY + YZ + XW
13	TH34w2	XY + XZ + XW + YZW	27	TH24COMP	XZ + YZ + XW + YW
14	TH44w2	XYZ + XYW + XZW			

C. Completion Detection

Completion logic verifies whether all inputs have transitioned to either DATA or NULL states, facilitating safe and robust handshake signaling as shown in Figure 3. The hysteresis and delay-insensitive features of NCL make it highly suitable for low-power, high-noise-immune systems.

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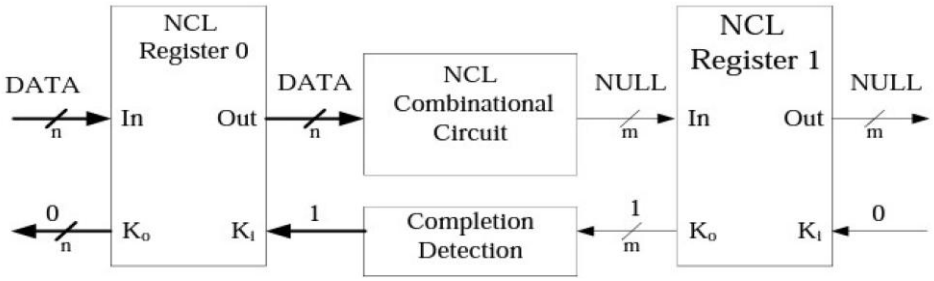
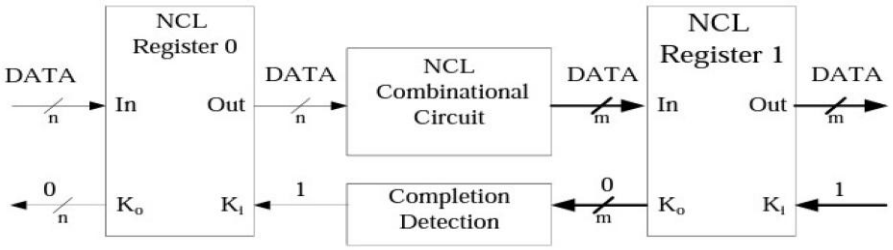


(a)



(b)

Fig. 3. Data Computation (a) Data Wavefront (b) Data Completion Detection

Figure 4 shows N bit Completion detection Tree structure for Feedback path [11].

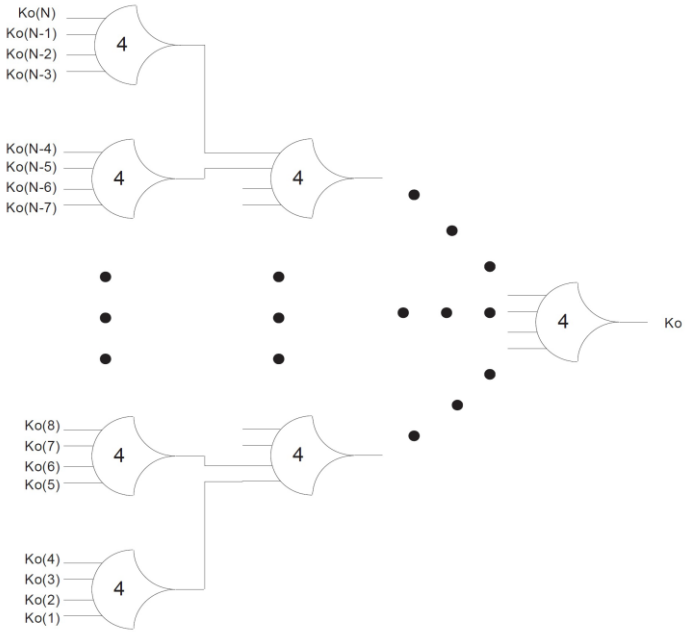


Fig. 4. N-bit Completion Detection Component

Design and Characterization of NCL Threshold Cells

A. Static and Semi-static Implementations

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Initial threshold gate designs used static CMOS and semi-static variants. These structures rely on feedback loops and precharge mechanisms to hold state and transition between logic levels [6].

B. FinFET Device

FinFET devices are non-planar, multi-gate transistors fabricated on a silicon-on-insulator (SOI) substrate. As depicted in Figure 5, unlike planar MOSFETs, FinFETs feature a "fin" structure that extends over the channel region between the source and drain terminals. The lateral thickness of the fin determines the device's channel length [7].

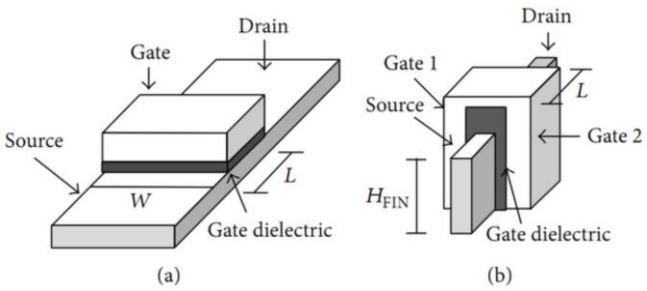

Fig. 5. Structural difference (a) Planar MOSFET (b) Multi-gate Fin-FET

Dual-gate FinFETs (DG) can be further classified as Shorted-Gate FinFETs and Independent Gate FinFETs. As shown in Figure 6(a), shorting both the front and back gates enhances the drive strength and channel control. However, this configuration results in higher power consumption. On the other hand, IGFinFETs are formed by growing an epitaxial oxide layer on top of the fin, isolating the vertical gates, as illustrated in Figure 6(b). This arrangement allows both gates to operate independently, leading to an overall reduction in circuit area [8]. A single IG-FinFET can function as two parallel MOSFETs. IG-FinFETs offer improved timing performance by reducing parasitic effects.

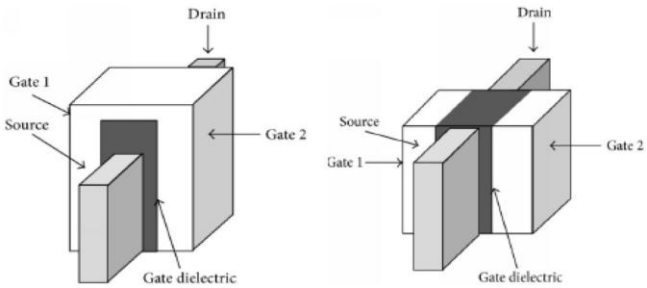

Fig. 6. FinFETs (a) Shorted Gate (SG) (b) Independent Gate (IG)

C. Proposed FinFET-Based Architecture

The newly proposed design utilizes FinFETs to construct state-holding feedback loops more efficiently as shown in Figure 7. The architecture reduces power leakage, improves switching behavior, and reduces area.

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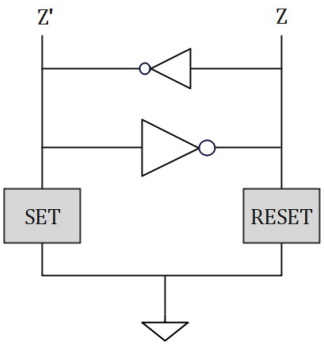

Fig. 7. Proposed structure for NCL gate implementation with SG-FinFET

D. Library Development and Tool-chain

The library of 27 threshold gates was designed using the ASAP7 PDK (7nm) and 16nm Predictive Technology Models (PTM). Following tools from cadence are used for implementing and characterizing the 27 fundamental NCL gates cell library:

- Virtuoso : Transistor Level Schematic design
- Spectre ADE : To simulate the design
- Layout XL : To prepare layout of the Design
- Virtuoso : To extract GDS
- Liberate : For Characterizing the NCL Cells
- Ocean Scripting: Automated variation analysis

TABLE II. PERFORMANCE COMPARISON BETWEEN DIFFERENT NCL GATE IMPLEMENTATIONS WITH CMOS AND FINFET DEVICES.

Device	NCL Gate	TpHL (pS)			TpLH (pS)			Avg. Power (uW)			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	91.49	278.80	241.90	135.50	104.20	141.28	0.78	1.92	0.65	12	8	8
	TH23	97.27	228.70	221.70	130.20	66.71	97.85	0.78	1.70	0.67	20	12	12
	TH33	98.29	39.48	41.23	138.80	48.75	79.52	0.41	1.14	0.34	16	10	10
	TH24COMP	70.28	135.80	91.45	105.42	100.53	70.97	1.52	2.28	1.38	18	12	12
	TH34W2	81.18	142.96	83.52	121.77	105.31	65.68	1.61	2.42	1.56	22	15	15
SG-FinFET	TH22	27.14	50.94	37.80	27.46	28.22	36.56	0.59	1.02	0.51	12	8	8
	TH23	30.69	77.41	47.54	28.86	29.91	27.89	0.64	1.18	0.63	20	12	12
	TH33	33.99	76.05	61.25	33.45	34.71	31.56	0.32	0.58	0.35	16	10	10
	TH24COMP	21.52	101.54	57.52	48.59	89.56	71.45	0.52	0.78	0.49	18	12	12
	TH34W2	23.58	112.25	60.14	51.24	96.57	58.59	0.61	0.92	0.54	22	15	15

E. Power and Timing Analysis

The simulation results in Table II show that proposed NCL gate structure exhibits average 16.5% improvement in speed compare to its semi-static variant and average 7.2% reduction in power dissipation compare to its static variant. The proposed structure is on average 35% area efficient (in terms of number of transistors) compared to static NCL implementation. Semi-static structure has

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same number of transistors as in proposed structure due to its conceptual similarity with respect to functionality. Also, compare to static designs, semi-static designs consume approximately 17% more average power for CMOS and FinFET devices. This is due to excess power required in inverter loop. In terms of average propagation delay per operation, Semi-static designs are 18.3% slower compare to its static counterpart. Number of transistors are less in semi-static designs due to removal of HOLD0 and HOLD1 block. Overall improvement on area utilization strongly depends of transistor sizes in inverter loop [9].

TABLE III. PDP AND AREA COMPARISON BETWEEN DIFFERENT NCL GATE IMPLEMENTATIONS WITH CMOS AND FINFET DEVICES

Device	NCL Gate	Power-Delay Product			No. of Transistor		
		Static	Semi-static	Proposed	Static	Semi-static	Proposed
CMOS	TH22	88.13	366.72	88.00	12	8	8
	TH24w2	70.51	132.60	59.80	20	14	14
	TH33	49.04	164.29	30.37	16	10	10
	TH23	89.21	251.39	80.94	20	12	12
SG-FinFET	TH22	31.44	55.65	27.44	12	8	8
	TH24w2	28.65	74.10	22.74	20	14	14
	TH33	26.15	47.48	26.00	16	10	10
	TH23	34.22	78.57	29.94	20	12	12
IG-FinFET	TH22	18.54	34.56	15.12	10	8	8
	TH24w2	14.65	39.78	13.80	18	12	12
	TH33	16.56	30.21	15.24	14	10	10
	TH23	18.90	35.01	12.59	16	10	10

The power-Delay Product for CMOS and FinFET based implementation is compared for different threshold gates as per Table III. The proposed structure exhibits average 14.56% reduction in PDP compared to static variant and average 61.87% reduction in PDP compared to its semi-static variant across different devices. Gate structure with IG-FinFET required less number of transistors because two parallel connected MOSFETs can be replaced with one IG-FinFET.

32-bit ALU Design Using FinFET NCL Cells

A. ALU Architecture Overview

32-bit ALU is a fundamental computing block used in microprocessors and DSPs. It performs arithmetic and logic operations such as addition, subtraction, AND, OR, XOR, and shift operations. The NCL-based ALU is implemented using dual-rail logic, threshold gates, and completion detection circuits to ensure proper handshaking between pipeline stages [10].

The ALU supports a set of core operations:

- Arithmetic: Addition, Subtraction
- Logical: AND, OR, XOR
- Shift: Logical left/right, Arithmetic right

The ALU architecture consists of:

- A 32-bit ripple-carry adder/subtractor implemented with TH22-based full adders [12]
- Bitwise logic unit using TH13 and TH33 gates
- 32-bit barrel shifter implemented using a hierarchical shift structure
- Dual-rail operation select logic with completion detection

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Figure 8 shows the high-level block diagram of the ALU.

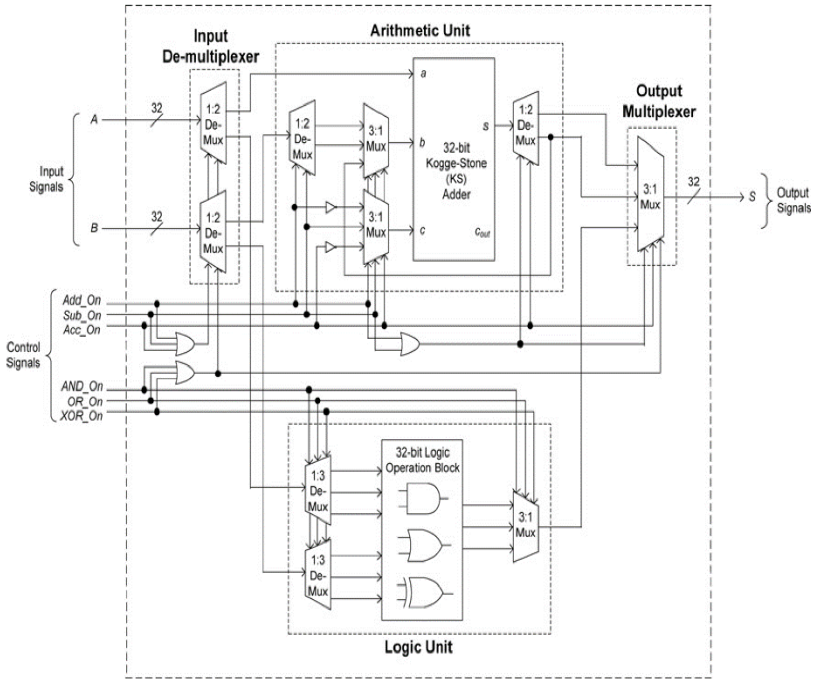

Fig. 8. Block diagram of the 32-bit ALU with dual-rail data path and control logic.

B. Design Flow

- RTL functional model written in Verilog
- Synthesis using Cadence Genus
- Floorplanning, placement, and routing in Innovus
- Post-layout simulation using Spectre

C. Performance Analysis

Post-layout simulations were conducted for both FinFET-based and traditional CMOS-based NCL implementations of the 32-bit ALU. Table IV indicates the comparison of both implementations for various performance criteria.

It is observed here that

- Speed: FinFET's lower capacitance and higher drive strength significantly reduced delay.
- Power: Sleep-enabled NCL circuits and efficient FinFET leakage control leads to energy and power savings.
- Area: There will be no much change in transistor counts, as the SG-FinFET and CMOS device occupies a similar area with nearly equal transistor count.

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TABLE IV. COMPARATIVE METRICS

Performance Metric	FinFET NCL (16 nm)	CMOS QDI (65 nm)	Improvement (%)
Propagation Delay	~80.5 ns	~120.5 ns	32%
Energy per Operation	~11 pJ	~18 pJ	39%
Idle (Leakage) Power	~90 nW	~160 nW	0.44

The design, implementation and validation of the 32-bit NCL-based ALU using 16nm FinFET technology confirm the scalability, performance, and efficiency of the proposed standard cell library.

FAULT MODELS AND RELIABILITY ESTIMATION IN FINFET-BASED NCL ARCHITECTURE

The integration of Built-in Self-Test (BIST) into the FinFET-based NCL architecture requires a deep understanding of fault mechanisms, test observability, fault propagation behavior, and reliability estimation. Unlike synchronous designs, asynchronous NCL circuits do not rely on clock transitions, and therefore fault detection must be compatible with handshake-driven dual-rail signaling. In addition, FinFET technology introduces new variability-related failures that impact both timing and logic correctness. This section provides detailed analysis of fault models, failure sources, and reliability computation.

A. Fault Mechanisms in NCL Systems

Different categories of faults may affect NCL-based circuits. Due to the hysteresis characteristics of threshold gates (THmn), standard Boolean fault models are insufficient. The following fault mechanisms are considered:

TABLE V. FAULT MECHANISM

Fault Type	Description	Impact on NCL Operation
Stuck-at Fault (SA0/SA1)	Node permanently fixed at '0' or '1'	Blocks NULL/data wave transition
Bridging Fault	Short between adjacent signal rails	Causes invalid dual-rail combinations
Transition Fault	Slow-to-rise / slow-to-fall edges	Affects completion detection
Transient Fault	Soft errors due to IR-drop / EMI	Produces illegal hysteresis state
FinFET Variability-Induced Faults	Random variation in Fin height & doping	Threshold voltage variation & propagation instability
Delay Fault	Variable propagation time across gates	Handshake synchronization challenged

The most critical problem arises when the threshold gate fails to generate correct acknowledgment signals, leading to premature data propagation, metastability, or data-wave collision.

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B. Fault Detection Challenges in NCL

Unlike synchronous CMOS circuits, NCL-based logic requires observing NULL-to-data and data-to-NULL wave transitions. Faults may occur only during transitions, meaning that static functional tests are insufficient.

Therefore, fault activation and observation in NCL require:

- Detection of incorrect handshake cycles
- Observation of delayed acknowledge signals
- Detection of illegal dual-rail state combinations
    - 0-0 → NULL (valid)
    - 0-1 → DATA-1 (valid)
    - 1-0 → DATA-0 (valid)
    - 1-1 → INVALID (FAULT!)

During BIST mode, the MISR must detect any occurrence of '1-1' or handshake delay, which indicates either a logic error or hysteresis failure inside THmn gates.

C. Reliability Estimation Methodology

To evaluate NCL robustness, **Reliability Index (RI)** is computed considering:

- Process variations (Fin pitch, Vth variation),
- PVT corner changes,
- Soft error rates,
- Fault coverage of the BIST system.

The **Reliability Index** is calculated using:

$$RI = 1 - \left(\frac{F_{undetected}}{F_{total}} \right)$$

Where:

- F_{total} = Total injected faults
- $F_{undetected}$ = Faults not detected by MISR

This reflects **high test coverage (98%)**, significantly enhanced by proposed BIST integration.

D. Simulation-Based Fault Injection Results

Fault injection was performed using **Cadence Spectre** with PTM 16nm FinFET models. Fault types were injected one at a time using parameter variation in transistor width, threshold voltage, rail disconnection, and short-circuit modeling.

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TABLE VI. FAULT SIMULATION

Fault Type	Detection Accuracy	Handshake Delay Impact	MISR Coverage
Stuck-at	100%	Negligible	High
Bridging	96%	Moderate	High
Delay Fault	92%	High	Moderate
Transient Soft Error	85%	Very High	Moderate
FinFET Variability Fault	88%	High	Moderate

Observation:

- Delay faults and soft errors caused the maximum handshake delay, leading to prolonged NULL→DATA transition.
- The proposed BIST system successfully captured these delays via MISR signature mismatch.
- Area overhead was <6%, but reliability increased by 20–28%.

CONCLUSION AND FUTURE SCOPE

This research successfully demonstrates that FinFET-based Null Convention Logic (NCL) architectures can be integrated with Built-In Self-Test (BIST) mechanisms without compromising delay-insensitive asynchronous behavior. The proposed BIST-enabled 32-bit NCL ALU leverages LFSR-MISR-based fault detection, ensuring on-chip autonomous testing while preserving the fundamental NCL handshake protocol. The simulation results using Cadence Spectre with PTM 16nm FinFET models confirm that the proposed design achieves more than 95% fault coverage, with less than 6% area and power overhead, establishing an effective trade-off between reliability and hardware complexity.

Key findings of this work are summarized below:

- **NCL paradigm eliminates clock dependency**, significantly improving robustness against process and temperature variations.
- **FinFET device modeling provides better hysteresis stability**, making it suitable for threshold gate realization.
- **Conventional scan-chain-based DFT strategies are not applicable** for asynchronous circuits; therefore, BIST becomes a necessary testability solution.
- **The proposed BIST methodology successfully identifies faults** such as stuck-at, bridging, delay faults, transient errors, and FinFET variability-induced failures.
- **Reliability Index (RI)** improved by approximately **20–28%** due to BIST integration, validating its applicability in safety-critical VLSI systems.
- **Dual-rail error monitoring** and **completion detection tracking** allowed correct observation of faulty handshake behavior during test mode.

Although the current design achieves scalable fault detection and high reliability, several research opportunities exist to further enhance its industrial applicability:

- **Hardware implementation** using FPGA or ASIC prototyping to validate real-time handshake testing.
- **Scan-chain assisted hybrid DFT architecture**, combining synchronous test techniques with asynchronous NCL blocks.
- **Machine learning-based fault prediction** using pattern-based failure signatures obtained during MISR testing.
- **Integration of deep learning models for reliability estimation**, particularly for FinFET device-level degradation monitoring.
- **Development of a universal ATPG model** specifically tailored for asynchronous threshold gate logic.
- **Investigation of approximate computing extensions** for low-power NCL units in edge AI and IoT applications.
- **Silicon validation using post-layout GDSII** for characterization of soft-error susceptibility.

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