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Research Article

Grid-Tied Power Quality Improvement Using a Five-Level Asymmetric Inverter-Based Unified Power Quality Conditioner

Rekha B*[1], Dr. Ramesh H R[2]
*[1]Research Scholar, Department of Electrical Engineering University Visvesvaraya College of Engineering K R Circle, bangalore 50001, India. *Email: rekha5reks@gmail.com
[2] Professor, Department of Electrical Engineering, University Visvesvaraya College of Engineering K R Circle, bangalore 50001, India.

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ABSTRACT

High-power, high-voltage applications frequently employ multi-level inverters (MLI) because of their superior performance over conventional five-level inverters. They provide higher DC link voltages, less electromagnetic interference, and less harmonic distortion. Higher component counts, issues with voltage balancing, and intricate pulse-width modulation control methods are some of the drawbacks of the current MLI. With fewer switches and a lower cost, this study suggests a five-level asymmetric inverter design that can produce a sinusoidal waveform with less harmonic content. A battery and photovoltaic (PV) system support the inverter's DC connection voltage. For UPQC control, sophisticated control techniques are used that make use of fractional order proportional integral resonant and fractional order proportional resonant controllers. A long short-term memory (LSTM) neural network is used to dynamically improve these controllers based on load and source nonlinearity, modifying the controller gains in real time. The performance of this suggested approach is verified by implementing it in the Matlab/Simulink tool.The results validate the superiority of the proposed strategy over existing methods in terms of sag compensation and harmonics reduction.Using the suggested control technique of a unified power quality conditioner (UPQC), the results verified that the proposed inverter had a total harmonic distortion (THD).

Keywords: Multi-level inverter,Unified power quality conditioner, Dynamic Voltage Restorer, Distribution Static Synchronous Compensator, fractional order proportional integral derivative, PV system.

1. Introduction

Due to the improved attributes and advancements in semiconductor technology, MLI is used in power electronic devices such as power converters and non-linear loads in power distributed systems [1]. These devices paved the way for significant improvement in power quality. The non-sinusoidal waveform flows from the load to the supply system via the grid, resulting in a significant voltage drop [2] in the transmission system as a result of the non-linear load.Improving power quality by lowering voltage sag, swell, harmonics, imbalanced, non-linear, and current levels can have a positive effect on the system's overall performance [3, 4]. Hence, tomitigate these effects,a flexible alternating current transmission system [5] is used. Some of them are Distribution Static Synchronous Compensator (DSTATCOM),Dynamic Voltage Restorer (DVR), thyristor switches series capacitors,UPQC[6-8],etc. The DSTATCOM [9, 10] provides compensating output when a high oscillation isoccurred onthe load side. In contrast, the DVR [11, 12] provides the compensating voltage when the supplied voltage is affected by uncertainty and harmonics. On the other hand, a DC link capacitor coupled to a power electronic circuit containing of a shunt and a series compensator is recommended for the UPQC [13, 14] in order to achieve both benefits in a system. This circuit will address power quality issues related to voltage and current.

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Nowadays, the power distribution system is made up of renewable resources due to its economic and eco-friendly operation. Meanwhile, the large scale penetration of renewable sources will impact the stable voltage flow of the perdistribution system [15]. Hence, it is essential to use renewable sources for an inverter circuit.Conventional voltage source inverters require large line filtersand high voltage rating based transistors, which makes the topology expensive [16]. Also, the converters make sure the output waveforms aren't sinusoidal. The goal of designing multi-level inverter topologies is to reduce the harmonic content in the output current [17]. The multi-level inverter can offer low switching loss and voltage jump, sinusoidal output waveform, reduce the size of the filter, and generate highly efficient output [18, 19]. Some examples of multi-level inverters are flying capacitors, cascade h-bridges, and diode clamped inverters [20].
The diode clamped inverter design, in contrast, makes use of large clamping diodes; the flying capacitor, on the other hand, requires a massive, rechargeable capacitor. This leads to the widespread use of cascade h-bridge inverters. However, for the design of the cascade h-bridge inverter, the number of switches for three phase supply system is high. However, the clamping circuit based inverter produces low harmonic contentfor the application of high power systems [21]. Hence, a clamping diode based multi-level inverter with reduced switch and other devices are used with the UPQC model. The multi-level inverter integrated UPQC model provides better control over injected reactive power from renewable resources. To address these concerns, this study offered a unique technique using controllers for improved performance. The main contributions of this proposed work are as follows.

- To improve the quality of power in the transmission system by using multi-level UPQC topology.
- To reduce the negative effects of non-linear load and source fault, an artificial intelligence based fractional order controller has been designed.
- To improve voltage regulation in hybrid renewable source based power systems through PV based power injection.

The remaining sections are arranged as follows: Section 2 describes the existing works related to power quality enhancement techniques in MLI. The proposed methodology and its system description aredescribed in section 3. Section 4 outlines the findings of the simulation outcomes, while Section 5 summarizes the final outcome.

2. Literature Survey

A high harmonic at the output current is a problem with the back-to-back converters of two-level inverters. In order to improve power quality, Thentral et al. [22] have reported a modular multi-level inverter based UPQC model. The model uses a seven-level inverter topology with field programmable gate array controller. The inverter sub-modules are constructed using half bridge topology with variable inner voltage levels. Both linear and non-linear loads are considered in the system analysis; however, the excessive number of switches makes the design both costly and inefficient. The inverter topology that was reported also has a large switching loss and current. Hence, a shunt active power filter and a thyristor-controlled series compensator were utilized in the adaptive power quality compensation system that Sindi et al. [23] developed. The compensation errors caused by both compensators are reduced using a proportional integral derivative controller. However, puzzle optimization was used to update the controller's gains in dynamic situations. The system was subjected to using PV, fuel cell, and battery storage unit jointly connected with a converter to supply AC voltage. Various line-to-ground faults, voltage imbalances, balanced sags, unbalanced sags, balanced swells, and unbalanced swells were used to test the system.
The disturbance encountered in the electrical network has a negative impact on the supplied power to the demand. Hence,Kenjrawy et al. [24] have used nine level structure of UPQC to supply sinusoidal power to the load. The adopted systemic model was controlled by a fuzzy logic controller concerning series and parallel converters. In order to acquire a control signal through fuzzy logic, synchronous reference frame theory-based conversions are used in conjunction with phase locked loops. Lastly, adaptive hysteresis band modulation was used to retrieve the converter's pulses. The reference voltage signal filter is utilized by the nine level adaptive hysteresis bands through the usage of a low pass filter. A neutral point clamped multi level inverter circuit was used by Chennai Salim et al. [25] for power quality enhancement. By utilizing a

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shared DC capacitor, the model employs a five-level inverter topology that integrates shunt and series active filters. Through the use of synchronous reference frame theory, the system's reference signal is derived. The signal was modulated by using level shifted sinusoidal pulse width modulation technique.

PV integrated UPQC system has been implemented by Ray et al. [26] for power flow analysis and power quality improvement. In order to provide strong convergence, the presented model employs an adaptive compensating model built on the variable leaky least mean square technique. Due to the use of that algorithm, the requirement of low pass and moving average filtering techniques is reduced. The PV is used as a DC supply of the voltage source converter part of the UPQC model. In order to manage the system's reference voltage and current, respectively, a proportional integral controller and a hysteresis current controller are introduced. The variable's weight was updated using the quadrature phase voltages of the source converters and the leaky least mean square algorithm. Table 1 depicts the summary of traditional methods.

Table 1. Overview of related works

Reference	Technique	Advantages	Disadvantages
Thentral et al. [22]	UPQC model	Enhancing power quality	High complexity
Sindi et al. [23]	puzzle optimization	Highly effective	Overfitting
Kenjrawy et al.[24]	UPQC	Enhanced reliability	Power consumption
Salim et al. [25]	UPQC	Cost effectiveness	Limited for power quality issues
Ray et al. [26]	UPQC system	More efficient power usage and reduced energy costs.	High initial cost

3. Proposed Methodology

Due to the environmental conditions, the power flows through the transmission line may be affected, resulting in power quality problems. This results in high distortion at the output voltage. Power systems use a lot of renewable energy sources to achieve economical and environmentally friendly operation. However, overall reactive power flow, loss, and stability of the system are not regulated, which leads to the use of a power conditioning system in the transmission line.

The voltage source of the system is accomplished by a hybrid source of wind turbine and tidal turbine. In a hybrid renewable system, the unregulated and defective voltage supply is an issue, even when the load is fed by AC voltage. Improving the integrated renewable system's power quality is possible with the use of a UPQC. To mitigate the load-side power quality issue, the conditioning unit that was adopted makes use of a DSTATCOM shunt compensator. The problems from the generator side are reduced by using a series of compensating devices of DVR. The traditional UPQC uses a voltage source inverter, which generates a square like waveform; moreover, the distortion in the output compensating voltage is high. Hence, to reduce that, a multi-level inverter that provides a sinusoidal waveform with reduced harmonic content is designed. Using fewer switches and more expansiveness, UPQC has settled on a five-level asymmetric inverter topology. Power from photovoltaic and battery systems powers the five-level asymmetric inverter's DC link voltage.Control of the five-level topologies is achieved by the use of fractional-order proportional-integral resonant and derivative controllers. The presented controllers are optimized or controlled utilizing extended short term memory, which is an addition of recurrent neural networks (RNN) based on the nonlinearity of the load and the source. The adopted artificial intelligence technique takes the load and source variations and jointly generatesthe gains of both controllers. Figure 1 represents the block diagram for the proposed work.

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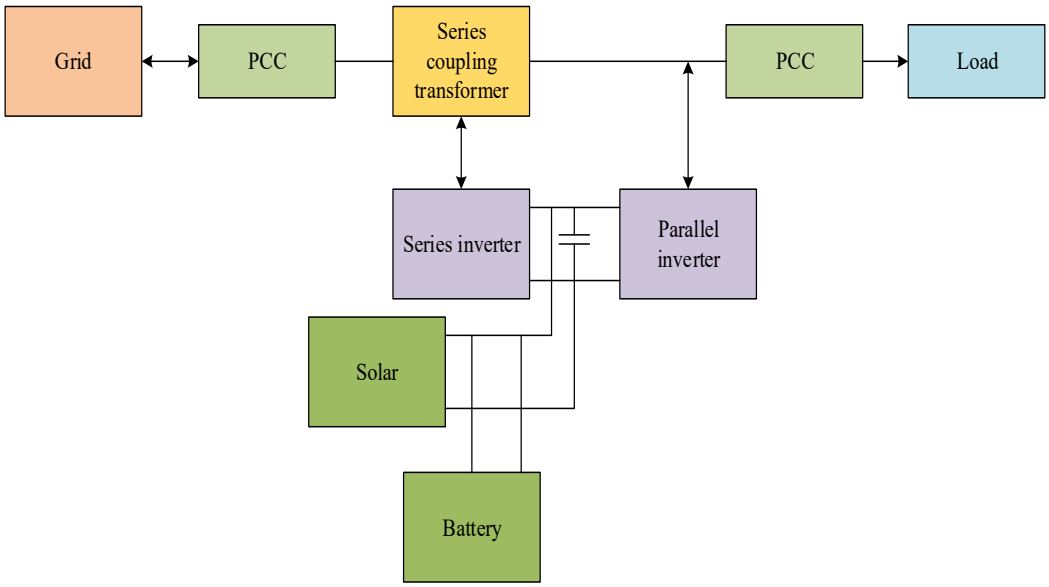

Figure 1: Block diagram for proposed work.

3.1 Photovoltaic System

Solar cell modeling is a crucial part of solar PV system analysis. Among the many solar cell models in use today is the single-diode model, also called the five-parameter mode [27]. Solar arrays are made up of different kinds of modules, each of which has multiple solar cells, which are basically semiconductor diodes (p-n). Climate and temperature are two of the main factors that affect how well a solar PV system works [28].

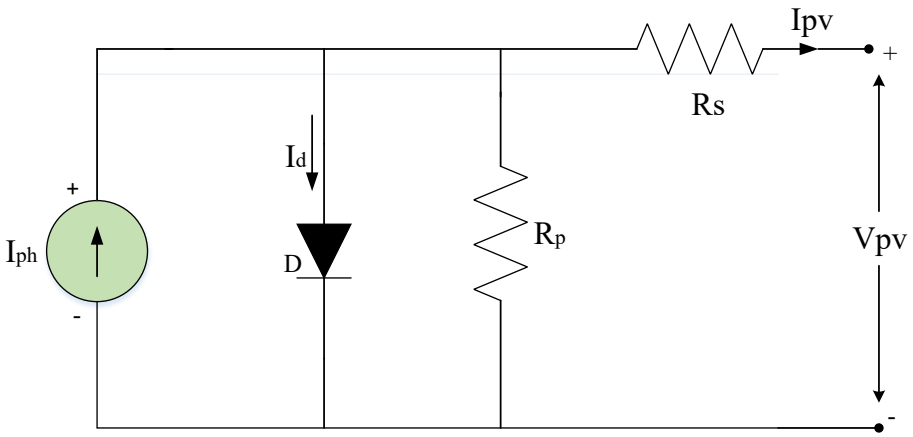

Figure 2: Equivalent circuit of PV system

The solar cell includes internal resistances R_{SE} *and* R_{SH} linked to the diode in a series and parallel configuration, respectively. Figure 2 shows the circuit comparable to a PV system model with a single diode. The solar cell produced current and voltage is mentioned as I_{PV} *and* V_{PV}. According to equation (1), the values are produced by linking many PV modules in series and parallel.

$$I_{PV} = \left\{ I_{ph} - I_O \left[\exp\left(\frac{q(V_{PV} + R_S I_{PV})}{N_{SE} AKT} \right) - 1 \right] - \frac{(V_{PV} + R_S I_{PV})}{N_{SE} R_{SH}} \right\} \quad (1)$$

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The PV cells linked with parallel and series are denoted as N_{SH} *and* N_{SE}, respectively. The resistance of the series is mentioned as R_S, and the parallel is expressed as R_{SH}. The ideal factor is given as A for the semiconductor device. K represent Boltzmann's constant and T is the temperature.
This implicit and non-linear equation (2) describes the I-V characteristic of the solar cell.

$$I = I_L - I_O\left[\exp\left(\frac{V + IR_S}{nV_T}\right) - 1\right] - \frac{V + IR_S}{R_{sh}} \qquad (2)$$

Where, I_L represent the light current (A), I_O is the diode reverse saturation current (A), V_T denotes variation of temperature, the resistance for series and shunt is articulated as R_s and R_{sh} in Ω, and the factor for the ideal diode is mentioned as n.

3.2 Battery Modelling

Power converters that can convert DC from batteries to AC with various voltage levels are known as battery multi-level inverters. Internal resistance R and a voltage source V, which stands for the open circuit voltage, make up this equivalent circuit model [29]. The battery's output voltage is the result.

$$V_{baty} = V - RI_{baty} \qquad (3)$$

Where, V_{baty} *and* I_{baty} depends on the battery's state of charge (SOC), temperature, and variations in internal resistance.
This study finds that a battery-based simplified model is adequate for assessing power management goals and comparing different strategies' performance [3]. One way to express the SOC over time (t) during charging and discharging is given below.

$$SOC(t) = \begin{cases} SOC(t-\Delta t) + P_{baty}.\dfrac{\eta_{ch}}{C_n.V_{dc}}.\Delta t \\ SOC(t-\Delta t) + P_{baty}.\dfrac{1}{\eta_{dis}.C_n.V_{dc}}.\Delta t \end{cases} \qquad (4)$$

The step of time is expressed as Δt, for battery, the power is denoted as P_{baty}, and the capacity of nominal is represented as C_n. The efficiencies during the charging and discharging phases are represented by η_{ch} *and* η_{dis} respectively. The DC bus voltage for nominal is expressed as V_{dc}. These limitations apply to the SOC regardless of when the step Δt occurs.

$$SOC_{\min} \le SOC(t) \le SOC_{\max} \qquad (5)$$

Where $SOC_{\min}$ *and* $SOC_{\max}$ represent the minimum and maximum permissiblestoringcapabilities, individually.

3.3 Unified power quality conditioner

A UPQC is a flexible tool that simultaneously reduces grid-side voltage disturbances and load-side current disturbances. The proposed method is built to operate loads using multiple feeders and linear loads. In UPQC, a custom power device connected between feeders is used to mitigate the issues while connecting various loads. Figure 3 depicts the design of the interline UPQC. A shared DClink connects the series and shunts active power filters. Shunt active power filters are reconnected backward, and the DC link is connected to a series of capacitors.

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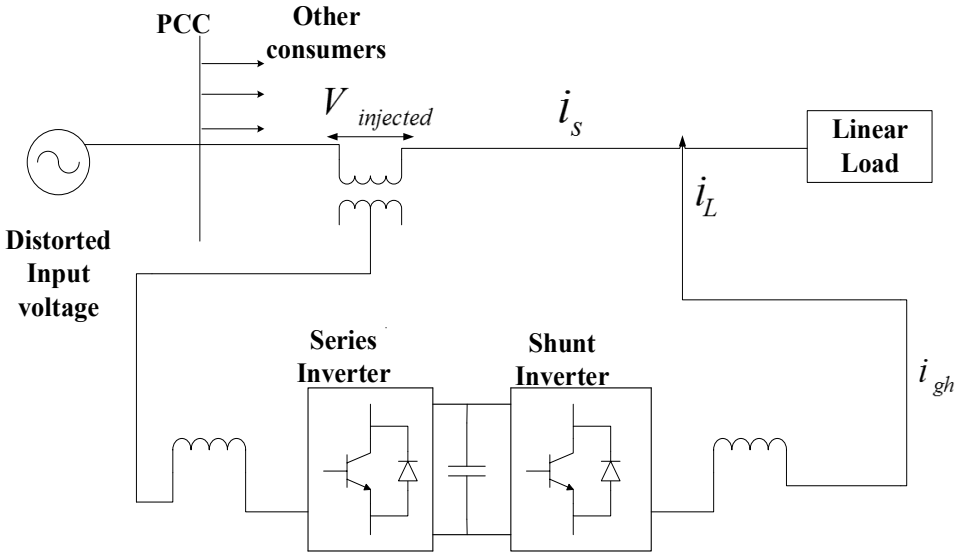

Figure 3: Line diagram of UPQC

By utilizing the point of common connection (PCC), shunt converters can be linked in parallel. The voltage and shunt filter current in UPQC-organized systems are provided by series filters. When working with voltage and current signals, UPQC can fix the PQ issues in independent MG systems. The primary function of a shunt converter is to reduce the harmonic content of the load current and modulate the DC link voltage. The primary function of a shunt D-STATCOM controller is to introduce reactive power into the grid at the PCC. When reactive current is not derived from the source, it is feasible to achieve a power factor of one. The reference current should be determined solely by the source's genuine power and losses. The DVR is implemented to mitigate network voltage surges and sag.

3.3.1Dynamic Voltage Restorer (DVR)

To mitigate fluctuations in either the balanced or unbalanced voltage, the dynamic voltage restorer injects the necessary voltage. It injects reactive power into the system while drawing active power from a DC power source [30]. When the network voltage is normal, the DVR stays in standby mode. It only activates when the voltage is abnormal. In the event of a power outage, the DVR automatically supplies the voltage differential between the lines to maintain the load side voltage at its nominal level. Overall, it is highly effective for protecting critical loads by preventing sudden voltage changes.The system arrangement of DVR is given in Figure 4.

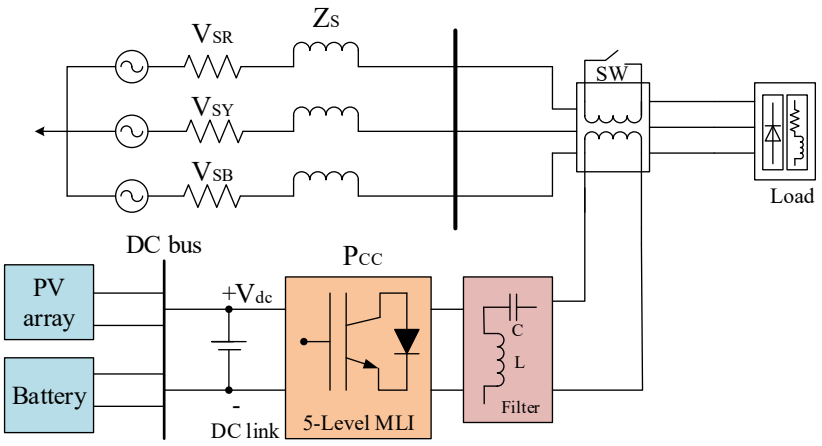

Figure 4: MLI-DVR configuration

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Injection transformers, a bypass thyristor, a voltage source inverter (VSI), passive filters, a protective circuit, and energy storage make up the DVR. When the voltage drops or rises, the DVR inserts a series voltage (V_{inj}) into the network through the transformer. This ensures that the load voltage remains at its designated value. The voltage that was injected is shown as follows.

$$V_L = V_S + V_{inj} \qquad (6)$$

Where, $V_L, V_S \; and \; V_{inj}$ denotes the load voltage, the injected voltage, and the sagged supply voltage correspondingly. When the voltage is normal, the load power for each phase is:

$$S_L = V_L I_L^* = P_L - jQ_L \qquad (7)$$

The loadpower for active and reactive is articulated as $P_L \; and \; Q_L$ through sags or swells and the current in load is mentioned as I_L. After the DVR restores a normal voltage level, the expression for equation (8) becomes clear:

$$S_L = P_L - jQ_L = (P_S - jQ_S) + (P_{inj} - jQ_{inj}) \qquad (8)$$

Where, P_S represent supply of power, P_{inj} denotes injected power, and Q_{inj} is the active and reactive injected quality.

3.3.2DSTATCOM Multi-level Inverter

A DC energy storage device, a coupling transformer, and a two-level Voltage Source Converter (VSC) make up the D-STATCOM. The distribution network is shunt-connected to this transformer [31]. A VSC divides the energy storage device's direct current (DC) voltage into three independent alternating current (AC) voltages. The coupling transformer's reactance aligns and phases these alternating current voltages with the AC system. Controlling the D-STATCOM's power exchanges with the AC system is as simple as adjusting the output voltages' phase and magnitude. Figure 5 illustrates the DSTATCOM system setup.

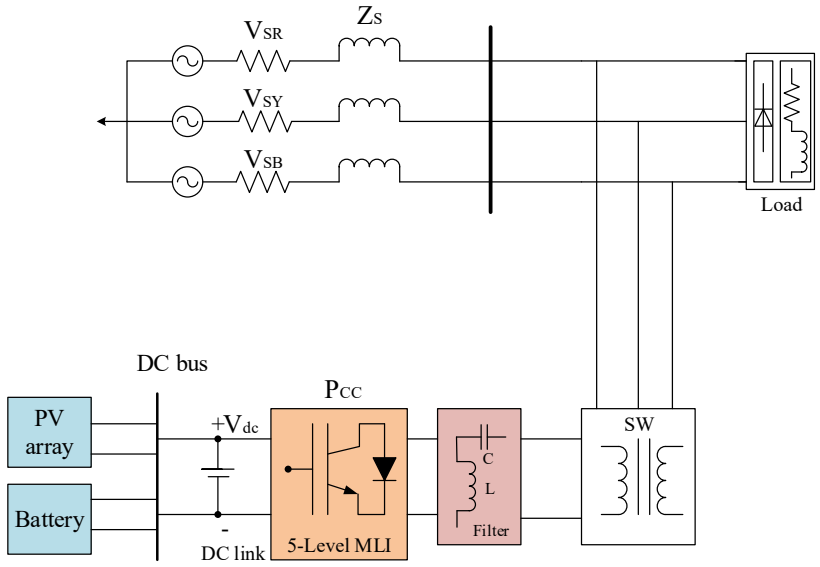

Figure 5: MLI-DSTATCOM configuration

The device can now either absorb or produce active and reactive power that can be measured due to this arrangement. The VSC offers a versatile topology that can be utilized for up to three separate purposes when linked in shunt with the AC system. In this instance, an indirectly operated converter is used to continuously regulate voltage using the device. One way to characterize the shunt-injected current I_{sh} is

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$$I_{sh} = I_L - I_S = \frac{I_L - (V_{th} - V_L)}{Z_{th}} \qquad (9)$$

$$\frac{I_{sh}}{\eta} = \frac{I_L}{\theta} \qquad (10)$$

The voltage dropthrough the system impedance Z_{th} is adjusted by the shunt injected current I_{sh}, which fixes voltage sag. The value of I_{sh} can be changed by modifying the converter's output voltage. A complicated power injection's D-STATCOM is as follows

$$Z_{sh} = V_L I_{sh}^{*} \qquad (11)$$

The voltage sag that D-STATCOM is able to rectify is conditional on the value of Z_{th} or the load bus fault level. By maintaining the injected shunt current in quadrature with V_L, the necessary voltage adjustment can be accomplished without the addition of any active power to the system. On the other hand, if I_{sh} is kept as small as possible, the system can adjust the voltage with very little apparent power injection.

3.45-Level multi-level inverter

Six separate DC sources, a utility grid, a five-level cascaded H-bridge inverter, and a filter make up the three-phase grid connection system seen in Figure 6[32].

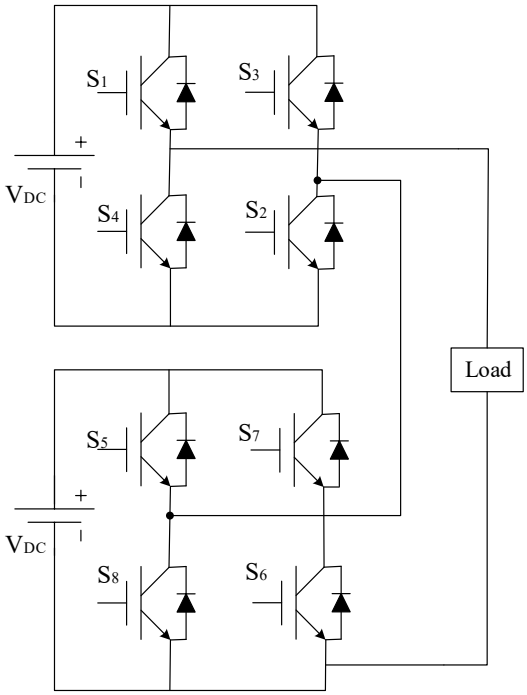

Figure 6:5-level MLI

Three independent CHBMLIs linked in a Y pattern make up the three-phase CHBMLI. There are two full bridges, or cells, in each phase, and they each have their own DC source. Every bridge consists of four IGBT switches, one of which has an anti-parallel diode. The advantageous properties of IGBTs over other types of power semiconductor switches led to their selection as the power semiconductor switches. The quantified output voltage level (L) is determined by the amount of cells (K) employed in a single phase.

$$L = 2K + 1 \qquad (12)$$

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The aggregate of the voltages produced by the cells corresponds to the overall voltage magnitude of the output for each phase. A voltage of -1V, 0V, or +1V can be generated by each cell. Hence, a 5-level inverter can produce DC voltages of-2V, -1V, 0V, +1V, and +2V as its output. The five-level inverter's switching state is shown in Table 2.

Table 2: Switching state of the five level inverter

Levels	Switches							
	S1	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**
$2V_{dc}$	1	1	0	0	1	1	0	0
V_{dc}	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
$-1V_{dc}$	0	0	1	1	0	0	1	1
$-2V_{dc}$	0	0	1	1	0	0	1	1

3.5Proposed FOPID-FOPR controller

The ordinary PID controller is generalized by the fractional-order PID (FOPID) controller [33]. The FOPID controller's transfer function in the Laplace domain is provided by:

$$H_{FOPID} = \frac{u(S)}{e(S)} = K_p + K_i S^{-\lambda} + K_d S^{\mu}; (\lambda, \mu > 0) \quad (13)$$

Equation (14) can be used to find a FOPID controller's time-domain control signal:

$$U(T) = K_p E(T) + K_i D^{-\lambda} E(T) + K_d D^{\mu} E(T) \quad (14)$$

From the above equation, the derivative, proportional, and integral gains are represented by K_d, K_p and K_i. The fractional orders of differentiation and integration are denoted by μ and λ .When compared to integer-order PID controllers, FOPIDs offer more design flexibility and robustness due to the incorporation of the tuning parameters μ and λ [34].The six control parameters that make up the Fractional Order Proportional Integral Resonant (FOPR) controller set it apart from other PR controllers [35]. Integrals and derivatives of fractional order can be used to improve the FOPR controller's performance. The system's resilience could be improved by making it more adaptable. Frequency domain analysis factors were considered when deciding to incorporate integral and derivative orders.The fractional integrator (FI) term exhibits $S^{-\beta}$ countless gain at $\omega = 0$ rad/s and offers reduced delay compared to a traditional integrator S^{-1} at high occurrences. For $0 < \beta < 1$, the phase shift delivered by $S^{-\beta}$ is α times smaller than that of a conventional integrator. As the value of β grows, the gain of the system improves for angular frequencies under 1 rad/s and decreases for occurrences over 1 rad/s. Beyond that, the FOPR controller's transfer functions in the Laplace (S) domain are produced by combining the S^{β} term with the conventional PR innovation. These transfer functions can be represented as below:

$$H_{FOPR}(S) = \frac{\omega_0 S^{\beta}}{S^2 + \omega_0^2} \quad (15)$$

$$H_{FOPR}(S) = \frac{\omega_0 S}{S^{\beta} + \omega_0^2} \quad (16)$$

$$FOPR(S) = K_p + K_I \frac{\omega_0 S^{\beta}}{S^2 + \omega_0^2} \quad (17)$$

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From the above equation, the fractional exponent of the FOPR controller is represented by S. The proportional term coefficient is indicated by K_p. The integral gain of the resonant term is represented by K_I. Figure 7 depicts the block diagram of the proposed cascaded FOPID-FOPR controller.

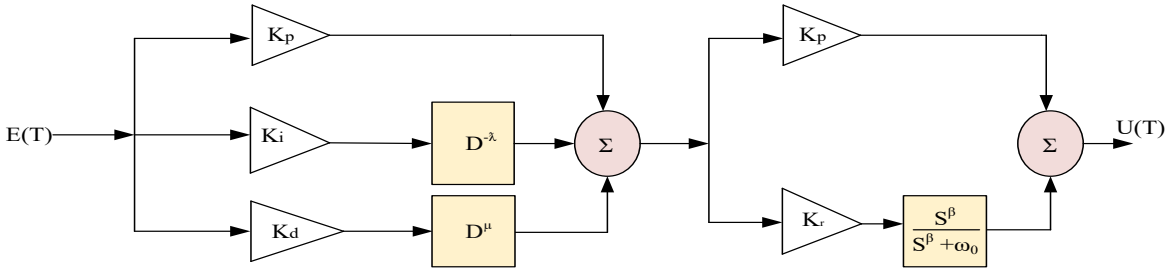

Figure 7: Block diagram of proposed cascaded FOPID-FOPR controller

3.6 Long short term memory (LSTM)

During the training process, the LSTM must learn to predict the value of the next time step for each input time step [36]. The sequence-to-sequence LSTM technique generates training sequences in which the values are moved by one time step. The input layer receives sequential data with a defined size and number of features and passes it on to the LSTM network layer. LSTM networks, a subtype of advanced RNNs, possess the additional capacity to retain information from the preceding step. A hidden state, input gates, forget gates, memory cells, and standard RNN-like forget gates make up an LSTM block.

The purpose of training an LSTM layer is to identify time series and sequential data with long-term dependencies among time steps. The amount of new values that enter the cell is controlled by the biases and weights associated with the input gate. In the same way, the biases and weights connected to the forget gate and output gate decide how much data is stored in the cell and used to figure out the LSTM block's output activation. Training the LSTM is done by feeding it sequences of data. The model is trained to anticipate sequence values one time step at a time, updating the network state following each prediction. The collection is made up of two parts: the test set and the train set. Initializing with the first data point, the network is trained using 90% of the full dataset. Then, it is tested using the last data point, which makes up 10% of the dataset. The standardization of the training data sequence to have zero mean and unity variance improves fitting and prevents training divergence. The following is the pseudo code that shows how to train an LSTM model to predict time series statistics.

Step 1: The input data sequences are loaded for testing and training.

Step 2: First, find the average and standard deviation of the training data. Then, use those numbers to create a standardized dataset that includes responses and predictors.

Step 3. Defining the LSTM network architecture

Step 4. Predict the future time steps

Step 5. The test data are standardized utilizing the same parameters as the training data

Step 6. Determine the unstandardized series of predictions using the standardized forecasts and the parameters from Step 2.

Step 7. Compute the loss function and validation.

If the actual values at each time step between forecasts are known, it is feasible to update the network state using observed values rather than ones that are predicted. Through the use of observed values rather than expected ones, this technique modifies the network state to yield more precise predictions. The MATLAB platform was utilized for this study to implement the forecasting of gain parameters.

4. Result and Discussion

The adopted UPQC model is executed in the Matlab/Simulink platform; thereby, the power quality of the supplied voltage is studied. The performance of the system for DVR, DSTATCOM, and the proposed UPQC device is analyzed. The Simulink model for the proposed work with various devices is shown in Figure 8.

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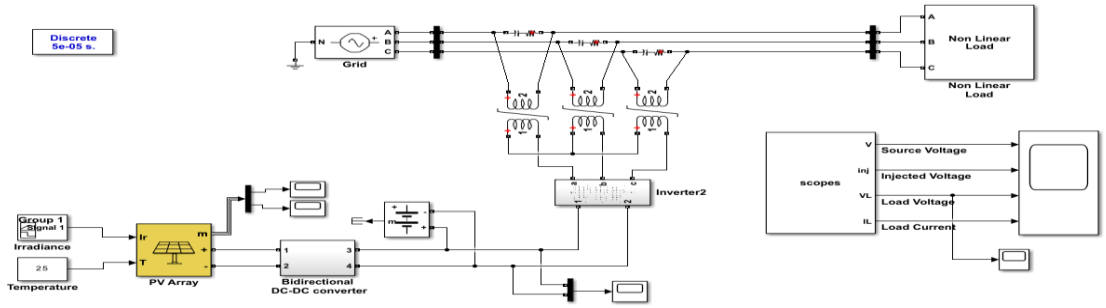
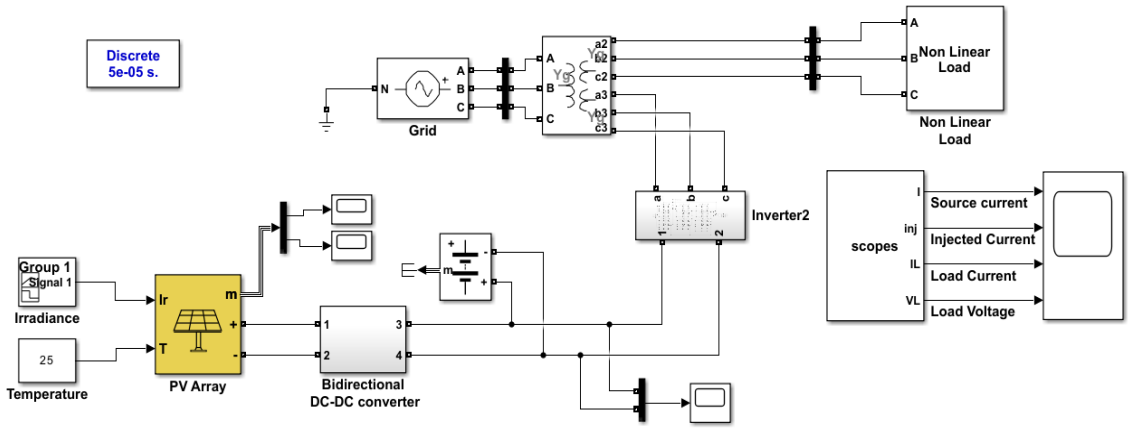
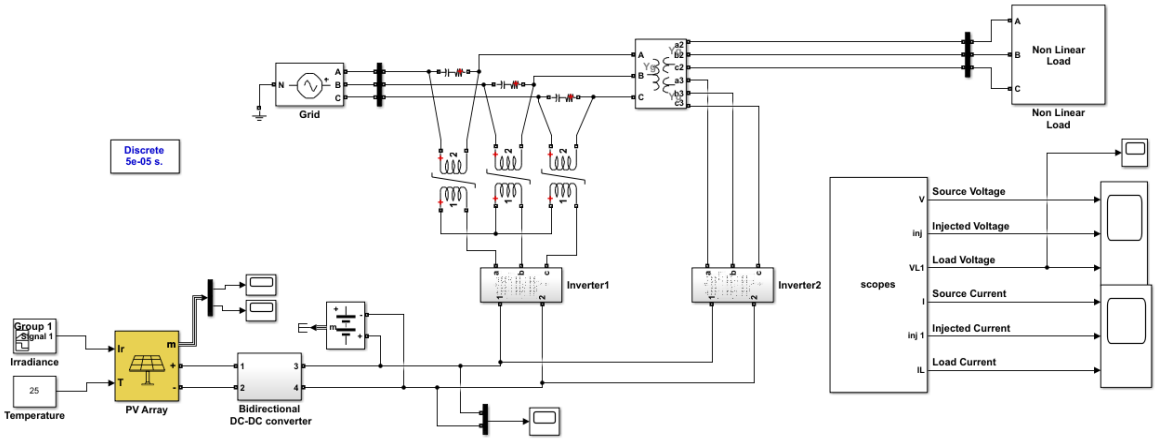
Since more power electronic switches are needed as voltage levels climb, the five-level inverter with DVR in Figure 8(a) is the ideal option for modeling. It is also important to think about different kinds of DC-DC converters, such as those that can be linked to a PV array. In Figure 8(b), a three-phase voltage source, connected with source impedance, is used to determine the supply voltage. The DSTATCOM is connected to the power source through the supply-to-shunt resistance and the point of common coupling (PCC). Figure 8(c) shows a three-wire, three-phase UPQC connected to a non-linear load's power supply. One AF series inverter and one AF shunt inverter each comprise the Active Filter (AF). Both inverters use the same DC link. Three one-phase transformers with a one-to-one ratio are used to link the supply and load terminals to the series filter. These transformers have a dual purpose: they inject voltage and filter out the series AF switching ripple.



(a)



(b)



(c)

Figure 8: Simulink model for the proposed work with (a) DVR, (b) DSTATCOM, (c)UPQC

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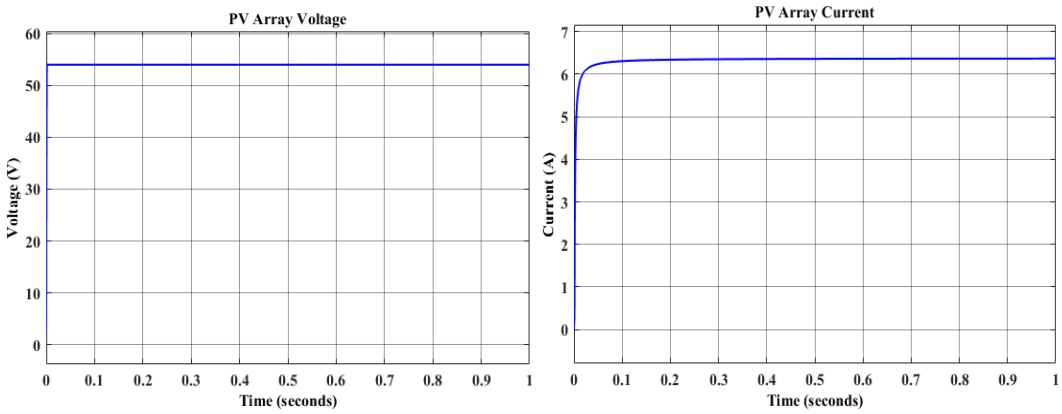

(a) (b)

Figure 9: Analysis of (a) PV array voltage and (b) PV array current

Figure 9 displays the analysis of the voltage and current derived from the PV array. The experiment primarily focused on evaluating the performance of a grid-connected solar photovoltaic (SPV) system under controlled conditions of constant irradiance and temperature. The irradiance level was maintained at 1000 W/m² while the temperature remained constant at 25°C. In this system, the output of the PV array voltage stabilized at 55 volts, while the PV array current settled at 6.2A.

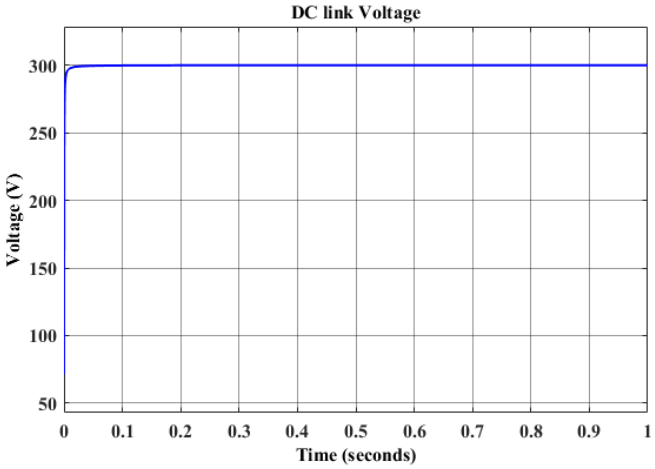

Figure 10: DC link voltage

Figure 10 depicts the DC link voltage. In this figure, the DC-link voltage exhibits a steadfast constancy throughout. This stability is achieved through both the PV power system and the battery system. The PV power system and battery contribute to the DC link voltage, ultimately achieving a stable output of 300 volts. The results showed that the DC-link voltage remains reliably constant, facilitating smooth and efficient operation within the system.

The inverter's output voltage and current are shown in Figure 11(a). The proposed system is connected with a three-phase load, indicating its capability to supply power to devices operating on a three-phase electrical system. To facilitate this, a three-phase inverter is employed. The three-phase inverter produces a voltage output of 350V. The three-phase inverter has an output current of 10A. Figure 11(b) shows the multi-level inverter's output voltage and current in a zoomed-in view.

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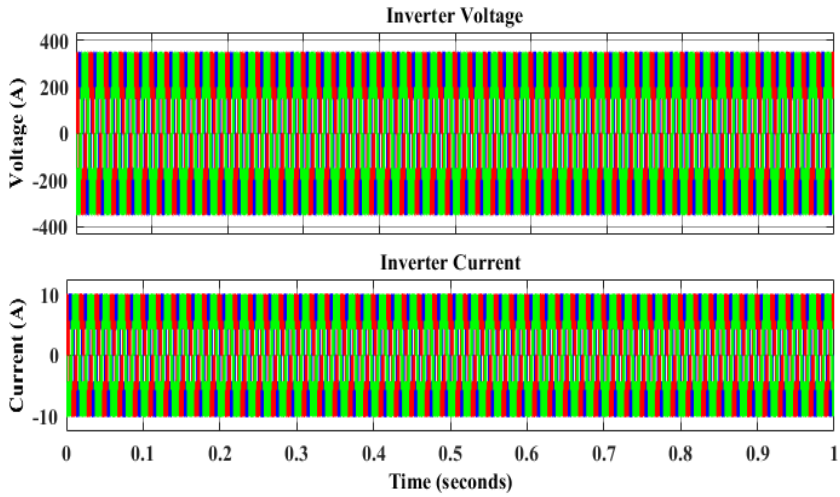
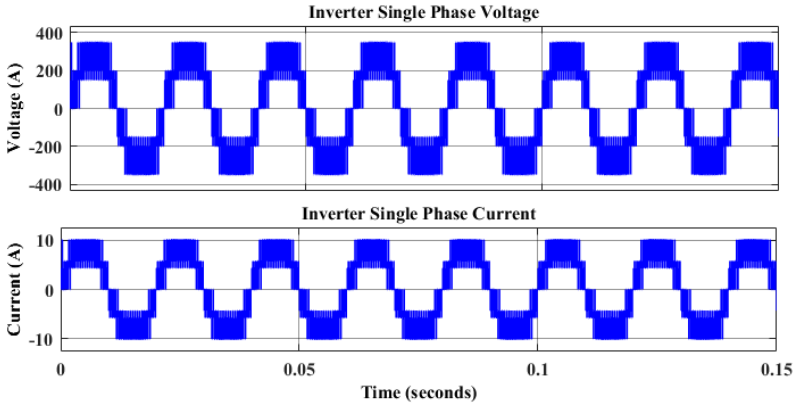


(a)



(b)

Figure 11. Output voltage and current of inverter

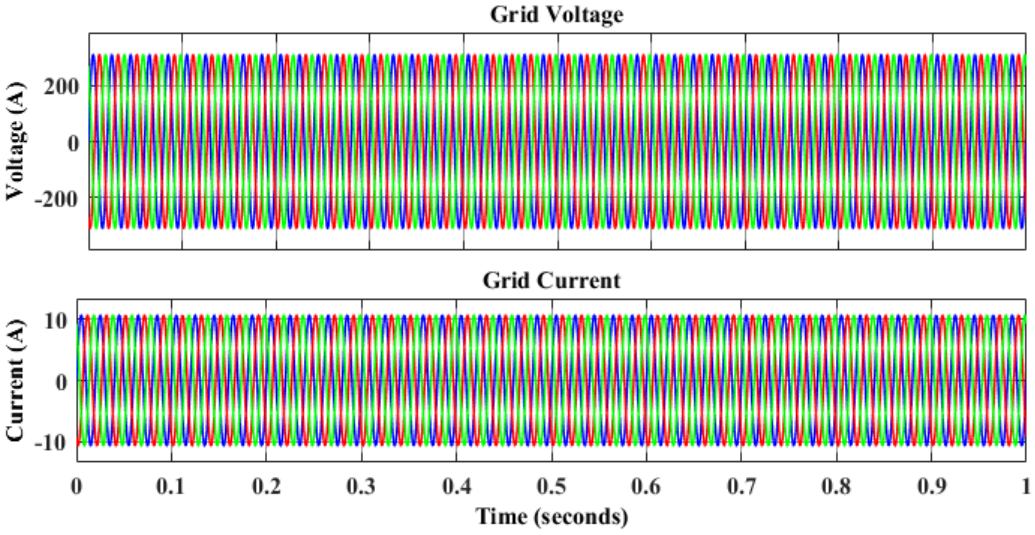


Figure 12. Grid voltage and Grid current

Figure 12 displays the grid voltage and grid current. The grid voltage and injected current are in phase because of the unity power factor. Grid voltage and grid current are constant when irradiance is constant.

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Specifically, the grid voltage maintains a stable output of 230 volts while the grid current remains consistently at 10A.

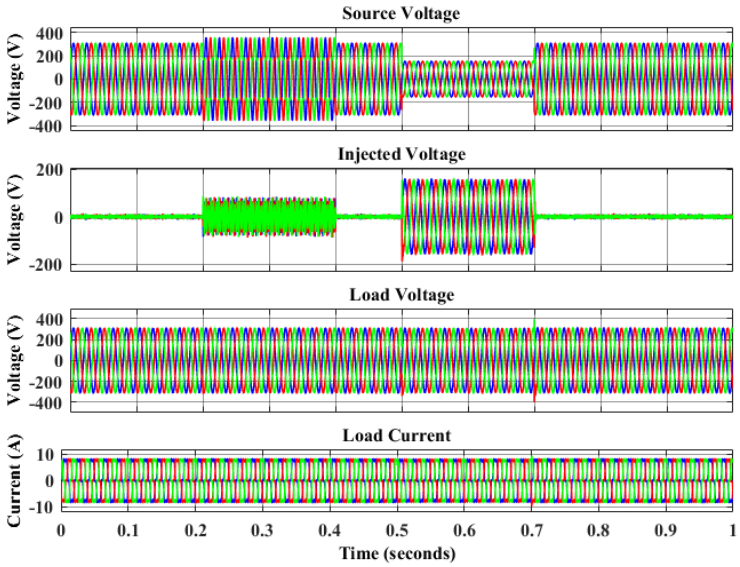

Figure 13: Simulation results with DVR

Figure 13 displays the three-phase source voltage with sag, the load voltage, the voltage injected by the DVR, and the source and load current. In relation to the load point reference voltage, a voltage sag of 0.5pu is applied throughout this test. The source voltage sag is induced by applying an overload during the time interval from 0.5 seconds to 0.7 seconds. The proposed DVR effectively injects the necessary voltages to maintain the load voltage profile.Additionally, a voltage swell is created at the same time interval (0.5 seconds to 0.7 seconds) to test the system's response. Both the load voltage and the DVR-injected voltage were present during the fault. The outcomes demonstrate how the suggested DVR mitigates balanced voltage sags to improve load circumstances, demonstrating the durability and efficacy of the DVR's operation.

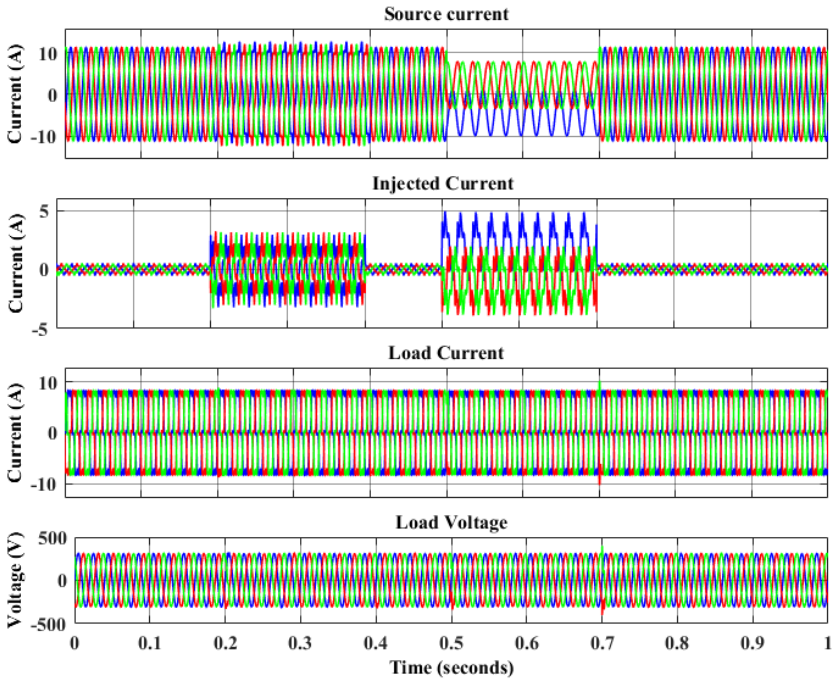

Figure 14: Simulation results with DSTATCOM

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Figure 14 shows the simulated response of the DSTATCOM. Initially, a source current swell occurs from 0.2 to 0.5 seconds, followed by a current sag from 0.5 to 0.7 seconds. During these intervals, the load current waveform becomes stepped and highly distorted, with significant triple harmonic components present. The voltage waveform is reduced, and the current is increased due to the injected current; the current swell and sag occur between 0.2 and 0.4 and 0.5 seconds, respectively. At t = 1 second, the DSTATCOM is activated, causing the source current waveform to become nearly sinusoidal and align closely with the source voltage waveform. As a result, the power factor of the voltage and current waveform approaches unity.

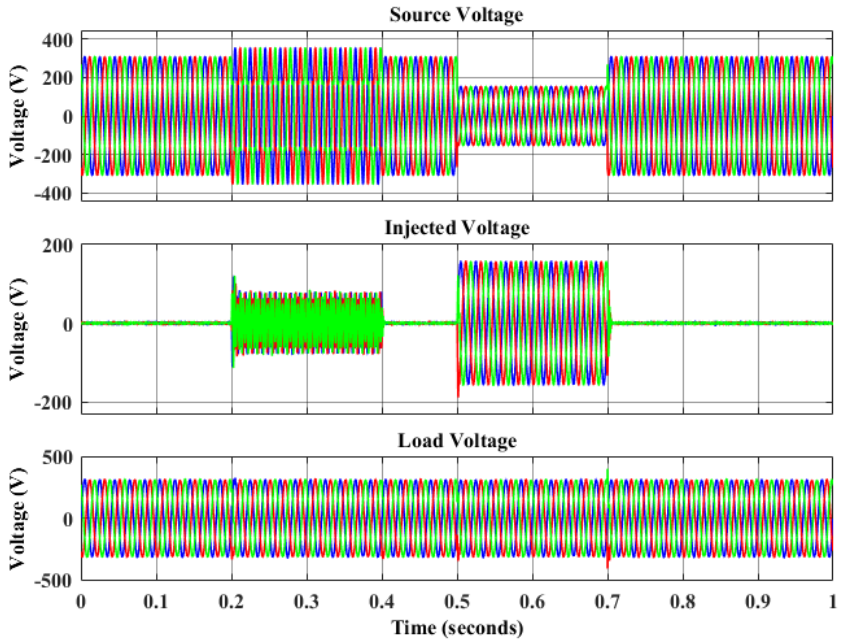

Figure 15: Simulation results for UPQC device

Figure 15 displays the three-phase source voltage with sag, the load voltage, and the UPQC injected voltage. During the span of 0.5 and 0.7 seconds, an overload is applied to cause the source voltage to drop. The source voltage increases when an overload is applied for 0.2 to 0.4 seconds.The proposed controller withUPQC effectively injects the necessary voltages to maintain the load voltage profile.The swelling and sagging of current and voltage lead to an increase in THD, resulting in power quality issues. Figure 16 shows the THD of a fundamental controller without the use of a UPQC, revealing a high THD of 0.73%. These fewer harmonics are obtained by using the proposed control strategy.

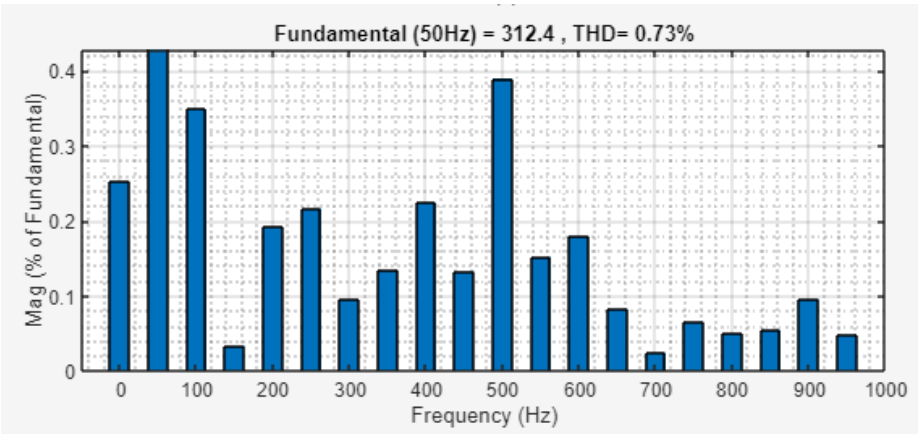

Figure 16: THD analysis

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Table 3: Comparative analysis of THD

Controller	DVR	DSTATCOM	UPQC Dvrdstatcom
FOPID	1.10%	1.13%	1.02%
FOPR	1.00%	1.08%	0.98%
Proposed Fopidfopr	0.84%	0.93%	**0.73%**

Table 3 compares the THD obtained from DVR, DSTATCOM, and UPQC systems. It demonstrates the efficiency of the proposed controller, which results in significantly less distortion than conventional methods. Additionally, the reduced number of devices in this approach decreases both the size and cost of the system.This comparison clearly demonstrates that the UPQC is more effective in reducing harmonics than the proposed controller.

5. Conclusion

This study uses a control system that integrates the cascaded FOPIR-FOPID controller with a five-level UPQC architecture. LSTM networks, a sophisticated kind of RNN, are used to improve and fine-tune the suggested controllers. A mix of solar and battery systems provide the DC link voltage for the five-level asymmetric inverter. To confirm its functionality under dynamic load variations, a real hardware prototype is made and put through testing in the lab. At the same time, simulations are carried out using MATLAB/Simulink. According to the trial findings, the suggested system with the UPQC device had a lower THD than DVR and DSTATCOM. The adjustment factor will be adjusted in the future to reduce errors and improve the hybrid algorithm.

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